



**JECRC<sup>TM</sup>**  
**UNIVERSITY**  
**BUILD YOUR WORLD**

**JECRC University**

**School of Engineering and Technology**

**Course Structure and Syllabus**

**M. Tech.**

**VLSI & Embedded  
System**

**Academic Programs**

**(2019-2021 )**

JECRC University  
**Faculty of Engineering and Technology**  
**M.Tech. (VLSI & Embedded System)**

**Teaching Scheme**

**Semester-I**

<b>Code</b>	<b>Subject</b>	<b>Contact Hours L-T-P</b>	<b>Credits</b>	
MEE022A	Digital VLSI Circuit Design	4-0-0	4	C
MEE023A	Computer Aided Design for VLSI Circuits	4-0-0	4	C
MEE046A	Microcontroller System Design	4-0-0	4	C
MEE045A	Real Time Operating System	4-0-0	4	C
MEE026A	VLSI Design Lab	0-0-2	2	C
MEE048A	RTOS and FPGA Lab	0-0-2	2	C
MEE069A	Seminar	0-0-2	2	C
	<b>Total</b>	<b>16-0-6</b>	<b>22</b>	

**Semester - II**

<b>Code</b>	<b>Subject</b>	<b>Contact Hours L-T-P</b>	<b>Credits</b>	
MEE028A	Analog and Mixed Signal ICs	4-0-0	4	C
MEE030A	Advanced ASIC and FPGA Design	4-0-0	4	C
MES001A	Research Methodology	3-0-0	3	C
MEE030A	Embedded Systems and Applications	4-0-0	4	C
MEE032A	Embedded System Lab	0-0-2	2	C
MEE027A	System Modeling Lab Using Verilog / VHDL	0-0-2	2	C
MEE059A	Seminar	0-0-2	2	C
MES002A	Quantitative Techniques & Computer Applications Lab	0-0-1	1	C
	<b>Total</b>	<b>15-0-7</b>	<b>22</b>	

***Semester - III***

<b>Code</b>	<b>Subject</b>	<b>Contact Hours L-T-P</b>	<b>Credits</b>	
MEE039A	Testing & Testability of VLSI Circuits	Elective-I 4-0-0	4	S
MEE040A	Image Processing in VLSI Design			
MEE015A	Wireless and Mobile Ad-hoc Networks			
MEE038A	Embedded Communication Software Design			
MEE044A	Low Power VLSI Design			
MEE043A	System Level Design & Modeling	Elective-II 4-0-0	4	S
MEE041A	Robotics & Automation			
MEE017A	Advanced Artificial Neural Networks			
MEE025A	Synthesis of Digital Circuits			
MEE023A	VLSI System and Subsystem			
MEE053A	Advanced Microprocessor	Elective-III 4-0-0	4	S
MEE054A	Architecture of Digital Signal Processors			
MEE055A	Embedded Hardware			
MEE056A	Data Compression Techniques			
MEE009A	Advanced Digital Signal Processing			
MEE058A	Advanced Digital System Design			
MEE059A	Soft Computing			
MEE060A	Advanced Computer Architecture			
MEE061A	Design of Digital Control System	Elective-IV 4-0-0	4	S
MEE062A	Cryptography and Network Security			
MEE063A	Data Communication & Computer Networks			
MEE064A	Mobile Computing			
MEE008A	Digital Image Processing			
MEE066A	Nanotechnology			
MEE047A	Embedded Networks & Protocols			
MEE049A	Mixed Signal Embedded Systems			
MEE050A	Multiprocessors Systems-On Chip			
MEE067A	Dissertation Part – I	12	12	C
	<b>Total</b>	<b>28-0-0</b>	<b>28</b>	

### ***Semester - IV***

<b>Code</b>	<b>Subject</b>	<b>Contact Hours L-T-P</b>	<b>Credits</b>
MEE068A	Dissertation Part – II	0-0-0	28
	<b>Total</b>	<b>0-0-0</b>	<b>28</b>

### **Program outcomes (POs):**

PO1. Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2. Problem analysis: Identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3. Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4. Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5. Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6. The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7. Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, Manual for Affiliated / Constituent Colleges NAAC for Quality and Excellence in Higher Education 126 and demonstrate the knowledge of, and need for sustainable development.

PO8. Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9. Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10. Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11. Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12. Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

### Digital VLSI Circuits Design

#### Course Objectives:

1. This is an introductory course which covers basic theories and techniques of digital VLSI Circuit design in CMOS technology.
2. In this course, we will study the fundamental concepts and structures of MOS Transistor and designing digital VLSI Circuits, static and dynamic Power Dissipation, interconnect analysis, Propagation delays, MOS Inverters and their Characteristics.
3. The course is designed to give the student an understanding of the different Combinational circuit design, Sequential MOS Logic Gates and CMOS Dynamic Logic Circuits including their Transient Analysis, design steps and behavior.
4. The Course also covers the study of various semiconductor Memory like ROM, RAM with input/output Circuits and their leakage mechanism.

**Unit I MOS Transistor**-First Glance at the MOS device, MOS Transistor under static conditions, threshold voltage, Resistive operation, saturation region , channel length modulation, velocity saturation, Hot carrier effect-drain current Vs voltage charts, sub threshold conduction , equivalent resistance, MOS structure capacitance, CMOS logic.

**Unit II MOS Inverter, Switching characteristics & Interconnect Effects**- Delay Time, Interconnect Parasitic Capacitances, Resistance, RC Delays, Inductances, Gate Delays, Stage Ratio, Power Dissipation, CMOS Logic Gate Design, Transmission Gate, BiCMOS.

**Unit III Combinational Circuit Design:** NAND Gate, NOR Gate, Transient Analysis of NAND & NOR Gate. Sequential MOS Logic Gates: Behavior of Bistable element, CMOS latches & Clocked Flip-Flops, Clock Skew, Clocking Strategies.

**Unit IV CMOS Dynamic Logic Circuits:** Pass Transistor, 0 and 1 transfer, Charge Storage & Leakage, Voltage Bootstrapping, High Performance Dynamic CMOS Circuits: Domino CMOS Logic, NORA CMOS Logic, Zipper CMOS Circuits, TSPC Dynamic CMOS.

**Unit V Semiconductor Memories:** ROM, DRAM, SRAM, PLA, Cell, Leakage Circuit and Input/output Circuit.

#### Course Outcome (CO):

At the end of this course students will have:

CO1-Ability to understand MOSFET and their fabrication.

CO2- Ability to understand any combinational circuit analysis using MOSFET.

CO3-Ability to understand & analyse sequential MOS circuits

CO4-Ability to draw layout of any circuit.

CO5-Ability to understand hardware description language.

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

<i>Course Outcome</i>	Program Outcome												Program Specific Outcome		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
CO1	H		H		L			M			L			H	
CO2	L		L	H	M	L				H		L	L		M
CO3	L	M		H			L				L				H
CO4			L		H		H						H		
CO5	H	M					H							M	

H = Highly Related; M = Medium L = Low

**Text Books**

1. Jan.M.Rabaey., Anitha Chandrakasan Borivoje Nikolic, "Digital Integrated Circuits", Second Edition.
2. Neil H.E Weste and Kamran Eshraghian, "Principles of CMOS VLSI Design", 2nd Edition, Addition Wesley, 1998
3. Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital IC- Analysis and Design", 3rd Edition, Tata McGraw Hill.

JECRC University

Contact Hours(L-T-P) : 4-0-0

Computer Aided Design for VLSI Circuits

**Course Objective:**

*This course provides a survey of advanced techniques for solving computer aided design problems for a wide range of design styles. A technology independent description is followed to provide algorithms and techniques that are applicable for a wide range of fabrication process.*

**Unit I: Introduction to VLSI Design methodologies** - Review of Data structures and algorithms, Review of VLSI Design automation tools, Algorithmic Graph Theory and Computational Complexity, Tractable and Intractable problems, general purpose methods for combinatorial optimization.

**Unit II: Design rules:** Layout Compaction - Design rules, problem formulation, algorithms for constraint graph compaction, placement and partitioning, Circuit representation, Placement algorithms, Partitioning

**Unit III: Floor planning:** Floor planning concepts, shape functions and floorplan sizing, Types of local routing problems - Area routing, channel routing, global routing, algorithms for global routing.

**Unit IV: Simulation:** Simulation, Gate-level modeling and simulation, Switch-level modeling and simulation, Combinational Logic Synthesis, Binary Decision Diagrams, Two Level Logic Synthesis.

**Unit V: Modelling and synthesis:** High level Synthesis, Hardware models, Internal representation, Allocation assignment and scheduling, Simple scheduling algorithm, Assignment problem, High level transformations.

**Course Outcome (CO):**

At the end of this course students will have:

CO1 - Student is able to understand the concepts of and electrical properties of MOS technologies.

CO2 - Student is able to understand different types layout designing tools and floor planning methods used in chip design.

CO3 - Establish comprehensive understanding of the various phases of CAD for digital electronic systems, from digital logic simulation to physical design, including test and verification.

CO4 - Demonstrate knowledge and understanding of fundamental concepts in CAD.

CO5 - Demonstrate knowledge of computational and optimization algorithms and tools applicable to solving CAD related problems.

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

<i>Cours e Outco me</i>	Program Outcome												Program Specific Outcome		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	P O9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
CO1	M	H								M				L	
CO2	M	H						H					L	H	L
CO3			H	M	L				L						M
CO4				H	H						L		H		
CO5						H	H					H			M

H = Highly Related; M = Medium L = Low

**Text Books**

1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2002.
2. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.

### MICROCONTROLLER SYSTEM DESIGN

#### **Course Objectives:**

1. *The objective of this course is to teach students design and interfacing of microcontroller-based embedded systems.*
2. *The internal structure and operation of microcontrollers will be studied. The design methodology for software and hardware applications will be developed through the labs and design projects.*
3. *This course will cover the various structures of microcontroller like 8051, 8096 microcomputer, Motorola microcontroller, PIC microcontroller and arm controller.*
4. *High-level languages are used to interface the microcontrollers to various applications. There are extensive hands-on labs/projects. Embedded system for sensor applications will be introduced. Students will be expected to develop independence and learn much of the material on their own.*

**Unit I: 8051 MICROCONTROLLER** Architecture of 8051 - Signals - Operational features - Memory and I/O addressing -Interrupts - Instruction set – Applications - The software model – functional description – central processing unit pin descriptions – reduced instruction set computer concepts – bus operations – super scalar architecture – pipelining – branch prediction – the instruction and caches – floating point unit – protected mode operation – segmentation – paging, protection, multitasking, exception and interrupts, input/output .

#### **Unit II: 8096 MICROCOMPUTER**

8096 CPU Structure- 8096 Interrupts Structure- Interrupt Control - Priorities- Critical Register - Programmable Timers- Interrupts Density and Interval Considerations- Real Time Clock.

**Unit III: MOTOROLA MICROCONTROLLER** Instructions and addressing modes of 68HC11 – operating modes – hardware reset, interrupt system - parallel I/O ports – flats – real time clock – programmable timer – pulse accumulator – serial communication interface – analog to digital converter – hardware expansion – basic assembly language programming.

**Unit IV :PIC MICROCONTROLLER:** Central processing unit architecture – instruction set – interrupts – timers – memory – I/Oport expansion – inter integrated circuit bus for peripheral chip access – A/D converter – universal asynchronous receiver transmitter – advanced risc machine architecture – advanced risc machine organization and implementation, advanced risc machine instruction set, thumb instruction set, basic advanced risc machine Assembly language program, advanced risc machine central processing unit cores.

**Unit V: ARM CONTROLLER**

Architecture – Memory Organization – Pipeline and cache concepts – ARM (32 bit) Architecture - Instruction set and Assembly Language Programming - ARM instruction set and THUMB instruction set - Switching between ARM and THUMB instructions.

**Course Outcome (CO):**

At the end of this course students will have:

CO1- an ability to program a microcontroller to perform various tasks

CO2- an ability to interface a microcontroller to various devices.

CO3- an ability to effectively utilize microcontroller peripherals

CO4- an ability to design and implement a microcontroller-based embedded system.

CO5- Understanding of Embedded system, programming, Embedded Systems on a Chip (SoC) and the use of VLSI designed circuits.

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

Course Outcome	Program Outcome												Program Specific Outcome		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
CO1	M	H								M				L	
CO2	M	H						H					L	H	L
CO3			H	M	L				L						M
CO4				H	H						L		H		
CO5						H	H					H			M

H = Highly Related; M = Medium L = Low

**Text Books**

1. John B. Peatman, Design with PIC Micro controller, Pearson Education, 2003.
2. ARM processor data book.
3. 8051 Microcontroller & Embedded systems By Madizi M.A.
4. James W. Stewart, Kai X. Miao, "8051 Microcontroller, The Hardware, Software, and Interfacing", Prentice-Hall Career & Technology, (1993).
5. Jonathan W. Valvano Brooks/cole ,Embedded Micro Computer Systems, Real Time Interfacing, Thomson Learning (200

## **REAL TIME OPERATING SYSTEM**

### **Course Objectives:**

1. *The objective of the course is to teach what a real-time operating system (RTOS) is, how real-time operating systems are useful for measurement and control applications, and how they differ from standard general-purpose operating systems like Windows.*
2. *To explain the concept of a real-time system and why these systems are usually implemented as concurrent processes.*
3. *To describe a design process for real-time systems.*
4. *To explain the role of a real-time operating system.*
5. *To introduce generic process architectures for monitoring and control and data acquisition systems.*
6. *The Course also covers the study Distributed operating systems, Real time models and languages, Real time kernel Principles and application domains.*

**Unit I Review of operating systems** Basic Principles-system calls-Files-Processes - Design and implementation of processes- Communication between processes - operating system structures.

**Unit II Distributed operating systems** Topology-Network Types-Communication-RPC-Client server model-Distributed file systems.

**Unit III Real time models and languages** Event based - Process based-Graph models - Petrinet models - RTOS tasks - RT scheduling - Interrupt processing-Synchronization - Control blocks-Memory requirements.

**Unit IV Real time kernel** Principles - Polled loop systems - RTOS porting to a target Comparison and Study of RTOS - VxWorks and mCoS, Introduction to POSIX and OSEK standards.

**Unit V Rtos and application domains** RTOS for image processing - Embedded RTOS for voice over IP-RTOS for fault tolerant applications - RTOS for control systems.

### **Course Outcome (CO):**

At the end of this course students will have:

CO1- To present the mathematical model of the system.

CO2. To develop real-time algorithm for task scheduling.

CO3. To understand the working of real-time operating systems and real-time database.

CO4. To work on design and development of protocols related to real-time communication.

CO5- Apply formal methods to the analysis and design of real-time systems

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

Course Outcome	Program Outcome												Program Specific Outcome		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
CO1	M	H								M				L	
CO2	M	H						H					L	H	L
CO3			H	M	L				L						M
CO4				H	H						L		H		
CO5						H	H					H			M

H = Highly Related; M = Medium L = Low

**Text Books**

1. Hermann K, “Real time systems-design principles for distributed embedded Applications”, kluwer academic, 1995
2. Charles Crowley “operating systems - A design oriented approach” McGraw Hill

**References**

1. RAJ BUHR,DL Beily, “An introduction to real time systems” PHI,1999
2. CM Krishna,Kang G. Shin, “Real time Systems”, Mc Graw Hill, 1997
3. Raymond J.A., Donald L Baily, “An introduction to real time operating systems”PHI, 1999

**JECRC University**  
**Faculty of Engineering & Technology**  
**M.Tech. VLSI & Embedded System Semester I**  
**Contact Hours (L-T-P): 2 hrs per week**

**VLSI Design Lab**

***List of Experiments***

**S. No. Experiment**

VLSI based experiments using CADENCE / TANNER

1. Introduction of EDA Tools CADENCE / TANNER and analysis of design flow in EDA tools.
2. Design and simulation of CMOS inverter with tanner tool.
3. Design and simulation of CMOS AND/OR Gate using Tanner.
4. Design and simulation of CMOS NAND/NOR Gate using Tanner.
5. Design and simulation of CMOS XOR/XNOR Gate using Tanner.
6. Design and simulation of Half Adder/ Half subtractor using Tanner.
7. Design and simulation of Full Adder/Full Subtractor using Tanner.
8. Design and simulation of Operational Amplifier using Tanner.
9. Design and simulation of 2\*1MUX using Tanner.
10. Design and simulation of Half Adder using 2\*1 MUX using Tanner.
11. Design and simulation of 3:8 Decoder using Tanner.
12. Design and simulation of CMOS D Latch using Tanner.
13. Design and simulation of flip-flop using Tanner.
14. Design and simulation of 4-Bit Shift Register using Tanner.
15. Design and simulation of 3-Bit up-Counter using Tanner.

***Course Outcome (CO):***

At the end of this course students will have:

CO1-Ability to understand MOSFET and their fabrication.

CO2- Ability to understand any combinational circuit analysis using MOSFET.

CO3-Ability to understand & analyse sequential MOS circuits

CO4-Ability to draw layout of any circuit.

CO5-Ability to understand hardware description language.

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

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CO1	H		H		L			M			L			H	
CO2	L		L	H	M	L				H		L	L		M
CO3	L	M		H			L				L				H
CO4			L		H		H						H		
CO5	H	M					H							M	

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JECRC University  
Faculty of Engineering & Technology  
*M.Tech. in VLSI & Embedded System Semester I*  
Contact Hours ( L-T-P):- 2 hours per week

### **RTOS & FPGA Lab**

1. Introduction to RTOS System solution & tools.
2. Testing RTOS Environment and System Programming using Keil Tools ARM 7 Development Board (5004A) and perform the following experiment.
  - a. Study and analysis of interfacing of LED's
  - b. Study and analysis of interfacing of 10 bit Internal ADC
  - c. Study and analysis of interfacing of Pulse Width Modulation (PWM)
  - d. Study and analysis of interfacing of Universal Serial Bus (USB)
  - e. Study and analysis of interfacing of Four External Interrupts
  - f. Study and analysis of interfacing of Real Time Clock (RTC)
  - g. Study and analysis of interfacing of universal asynchronous receiver/ transmitter (Uart0) for transmission of data
3. RTOS System Solutions with Tornado tools.
4. Embedded DSP based System Designing.
  - a) Code compressor studio (CCS) for embedded DSP using Texas tool kit.
  - b) Analog DSP tool kit.
5. Simulation & Synthesis of the designs made using "VHDL / VERILOG and Mixed, of following digital circuits"
  - Combinational circuits:**
    - a. 8X1 MUX & 1X8 DMUX
    - b. 16X1 MUX using two 8X1 MUX.
    - c. ENCODER
    - d. DECODER
    - e. LED TO SEVEN SEGMENT DISPLAY
    - f. CARRY LOOK AHEAD ADDER
  - Sequential Circuits**
    - g. FLIP FLOP(D, R-S, J-K & T)
    - h. Counters
  - Advance Circuit Design**
    - 4 to 6-MSI Digital blocks (Combinational Circuits)
    - 6 to 8 MSI and 1 or 2 VLSI Circuits.(Sequential Circuits)

**Course Outcome (CO):**

At the end of this course students will have:

CO1- To present the mathematical model of the system.

CO2. To develop real-time algorithm for task scheduling.

CO3. To understand the working of real-time operating systems and real-time database.

CO4. To work on design and development of protocols related to real-time communication.

CO5- Apply formal methods to the analysis and design of real-time systems

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

<i>Cours e Outco me</i>	Program Outcome												Program Specific Outcome		
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CO1	M	H								M				L	
CO2	M	H						H					L	H	L
CO3			H	M	L				L						M
CO4				H	H						L		H		
CO5						H	H					H			M

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JECRC University

Faculty of Engineering & Technology

M.Tech. in VLSI & Embedded System Semester II

Contact Hours (L-T-P) : 4-0-0

Hours: 48

### Analog and Mixed Signal ICs

#### **Course Objective:**

*This course adopts a strongly industrial perspective and starts with a review of the important operating features of MOS devices. Functions addressed include primitive cells, biasing and references, op-amp designs, sampled and continuous time filters, A/D and D/A converters, clock generation systems for digital and mixed signal IC.*

**Unit I: Introduction to analog design:** Review of MOS Transistor operation models; Small signal model and large signal model; Single-Stage Amplifiers: common source stage; common source stage with resistive load; CS stage with diode connected load; CS stage with current source load; CS stage with source degeneration; Source follower; Common gate stage; Cascode Stage.

**Unit II: Differential Amplifiers:** single ended and Differential Operation, Basic differential Pair, Common mode response, differential pair with MOS load Gilbert Cell, Basic current Mirrors; Cascode Current mirror, Active Current mirrors; frequency response of amplifiers; miller effect, frequency response of CS stage, common gate stage, Cascade stage differential pair.

**Unit III: Theory and design of MOS Operational Amplifier:** performance parameters, One-stage Op Amps, Gain Boosting, Common Mode Feedback, Input Range Limitations, slew rate, power supply rejection Noise in Op Amps; Stability and Frequency Compensation, multipole systems, phase margin.

**Unit IV: Switched Capacitor Circuits:** Sampling switches; MOSFET as Switches, Speed considerations, Precision Considerations, Charge Injection Cancellation; Switched-Capacitor Amplifiers; unity gain sampler/Buffer, Non-inverting Amplifier; Switched-Capacitor Integrator; Switched-Capacitor Common-Mode Feedback.

**Unit V: Nonlinear Analog circuits:** Nonlinearity of different Circuits, Effect of negative Feedback on nonlinearity, Capacitor Nonlinearity, Linearization techniques; Oscillators; Ring Oscillators, LC Oscillators, Voltage Controlled Oscillators; PLL; Phase Detector, Basic PLL Topology, Dynamics of simple PLL.

#### **Course Outcome (CO):**

At the end of this course students will have:

CO1. Analyze and design op-amps, comparators, sample and hold circuits, switched capacitor circuits, non-linear analog circuits and data converters.

CO2. Design multi-stage MOS amplifier circuits to meet given specifications such as gain, frequency, power, and area specifications.

CO3. Use low-voltage, low-power design techniques for mixed-signal CMOS ICs.

CO4. Use electronic computer-aided design software (Mentor Graphics) to simulate and characterize circuits. The analog layout techniques will also be addressed.

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

<i>Course Outcome</i>	Program Outcome												Program Specific Outcome		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
CO1	M	H								M				L	
CO2	M	H						H					L	H	L
CO3			H	M	L				L						M
CO4				H	H						L		H		
CO5						H	H					H			M

H = Highly Related; M = Medium L = Low

**Text Books**

1. Behzad, Razavi: Design of Analog CMOS Integrated Circuits, MGH, 2001.
2. Allen Holberg: CMOS Analog Integrated Circuit Design, Oxford University Press, 2002.
3. P. R. Gray, Hurst, Lewis and R. G. Meyer. Analysis and Design of Analog Integrated Circuits. John Wiley, 4th Ed. 2001.
4. A. B. Grebene, Bipolar and MOS analog integrated circuits design. John Wiley, 1984.

JECRC University

Faculty of Engineering & Technology

*M.Tech. in VLSI & Embedded System Semester II*

*Contact Hours (L-T-P) : 4-0-0*

**Hours: 48**

**Advanced ASICs and FPGA Design**

**Course Objectives:**

1. Understand the different types of programmable logic devices, their architecture, routing and programming techniques,

2. Go through a complete ASIC design flow utilizing an FPGA and know the different CAD tools used at each level.

**Unit I Types of ASICs:** Design flow, CMOS transistors CMOS Design rules, Combinational Logic Cell, Sequential logic cell, Data path logic cell, Transistors as Resistors, Transistor Parasitic Capacitance, Logical effort, Library cell design, Library architecture .

**Unit II Programmable Asics, programmable ASIC logic cells and programmable ASIC i/o cells :** Anti fuse, static RAM, EPROM and EEPROM technology, PREP benchmarks , Actel ACT , Xilinx LCA , Altera FLEX, Altera MAX DC & AC inputs and outputs, Clock & Power inputs, Xilinx I/O blocks.

**Unit III Programmable ASIC interconnect, programmable ASIC design software and low level design entry:** actel act, Xilinx lca, Xilinx Epld, Altera max 5000 and 7000, Altera max 9000, Altera flex, Design systems, logic synthesis, Half gate asic, Schematic entry, low level design language, Pla tools, Edif, Cfi design representation.

**Unit IV Logic synthesis, simulation and testing:** Verilog and logic synthesis, VHDL and logic synthesis, Types of simulation, Boundary scan test, Fault simulation, Automatic test pattern generation, Introduction to JTAG.

**Unit V ASIC construction, floor planning, placement and routing:** System partition, Introduction to FPGA Architectures, FPGA design flow, Partitioning methods, Floor planning, Placement, physical design flow, Global routing, Detailed routing, Special routing, Circuit extraction and DRC.

**Course Outcome (CO):**

At the end of this course students will have:

CO 1: Continue discussion synthesis subset. Review finite state machines.

CO 2 Introduce ASIC design methodologies and synthesis tools, VHDL simulation and verification

CO 3: Discuss standard libraries. Introduce optimizations  
 CO 4 Introduce FPGA Synthesis tools and Intellectual Property Cores  
 CO 5 : Topics TBA, related to main project.

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

Course Outcome	Program Outcome												Program Specific Outcome		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	H		H			M			M	M	H	M		H	
CO2	H		H	M		H	M			H	M		M	H	M
CO3	H	M						H	H						H
CO4			M			H					M	H	H		
CO5	M	M							L			H			M

H = Highly Related; M = Medium L = Low

**Text Books**

1. Brown, S. D., Francis, R. J., Rose, J. and Vranesic, Z G. Field programmable Gate arrays. Kluwer, 1992.
2. Betz, V., Rose, J. and Marquardt, A. Architecture and CAD for Deepsubmicron FPGAs. Kluwer, 1999.
3. Trimberger, S. M. FPGA Technology. Kluwer, 1992.
4. Oldfield, J. V. and Dorf, R. C. FPGAs: Reconfigurable logic for rapid prototyping and implementation of digital systems. John Wiley, 1995.

**Research Methodology**

**Course Objective:**

- To gain insights into how scientific research is conducted.
- To help in critical review of literature and assessing the research trends, quality and extension potential of research and equip students to undertake research.
- To learn and understand the basic statistics involved in data presentation.
- To identify the influencing factor or determinants of research parameters.

<b>UNIT 1:</b>	<p><b>Research Methodology-Introduction</b>  Meaning of Research, Objectives of Research, Motivation in Research, Types of Research, Research Approaches, Significance of Research, Research Methods versus Methodology, Research and Scientific Method, Importance of Knowing How Research is Done, Research Process, Criteria of Good Research, Problems Encountered by Researchers in India</p>
<b>UNIT 2:</b>	<p><b>Defining the Research Problem</b>  What is a Research Problem?, Selecting the Problem, Necessity of Defining the Problem, Technique Involved in Defining a Problem</p> <p><b>Research Design</b>  Meaning of Research Design, Need for Research Design, Features of a Good Design, Important Concepts Relating to Research Design, Different Research Designs, Basic Principles of Experimental Designs</p>
<b>UNIT 3:</b>	<p><b>Sampling Design</b>  Census and Sample Survey, Implications of a Sample Design, Steps in Sampling Design, Criteria of Selecting a Sampling Procedure, Characteristics of a Good Sample Design, Different Types of Sample Designs, How to Select a Random Sample?, Random Sample from an Infinite Universe, Complex Random Sampling Designs</p> <p><b>Measurement and Scaling Techniques</b>  Measurement in Research, Measurement Scales, Sources of Error in Measurement, Tests of Sound Measurement, Technique of Developing Measurement Tools, Scaling, Meaning of Scaling, Scale Classification Bases, Important Scaling Techniques, Scale Construction Techniques</p>

<b>UNIT 4:</b>	<p><b>Methods of Data Collection</b> Collection of Primary Data, Observation Method, Interview Method, Collection of Data through Questionnaires, Collection of Data through Schedules, Difference between Questionnaires and Schedules, Some Other Methods of Data Collection, Collection of Secondary Data, Selection of Appropriate Method for Data Collection, Case Study Method</p> <p><b>Processing and Analysis of Data</b> Processing Operations, Some Problems in Processing, Elements/Types of Analysis, Statistics in Research, Measures of Central Tendency, Measures of Dispersion, Measures of Asymmetry (Skewness), Measures of Relationship, Simple Regression Analysis, Multiple Correlation and Regression, Partial Correlation, Association in Case of Attributes</p>
<b>UNIT 5:</b>	<p><b>Sampling Fundamentals</b> Need for Sampling, Some Fundamental Definitions, Important Sampling Distributions, Central Limit Theorem, Sampling Theory, Sandler's A-test, Concept of Standard Error, Estimation, Estimating the Population Mean (<math>\mu</math>), Estimating Population Proportion, Sample Size and its Determination, Determination of Sample Size through the Approach Based on Precision Rate and Confidence Level, Determination of Sample Size through the Approach Based on Bayesian Statics</p>

**Course Outcome (CO):**

At the end of the course, the student should be able to:

CO1 - Gain insights into how scientific research is conducted.

CO2 - Help in critical review of literature and assessing the research trends, quality and extension potential of research and equip students to undertake research.

CO3 - Learn and understand the basic statistics involved in data presentation.

CO4 - Identify the influencing factor or determinants of research parameters.

CO4 - assess critically the following methods: literature study, case study, structured surveys, interviews, focus groups, participatory approaches, narrative analysis, cost-benefit analysis, scenario methodology and technology foresight.

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

<i>Course Outcome</i>	Program Outcome												Program Specific Outcome		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	P O9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
CO1	M	H								M				L	

CO2	M	H						H					L	H	L
CO3			H	M	L				L						M
CO4				H	H						L		H		
CO5						H	H						H		M

H = Highly Related; M = Medium L = Low

Text Book: Research Methodology – Methods & Techniques by C. R. Kothari, New age International Publisher

**Notes for Examiner / Paper Setter:**

1. 1<sup>st</sup> Question shall be of 20 marks and compulsory for all. It may consist of Multiple Choice Questions (MCQ) of one mark each and short answer questions of one or two marks.
2. One question of 10 marks shall be set from each Unit which may have parts including numericals. Paper setter may give internal choice, if required.
3. Students will be required to attempt all questions compulsorily.

**Embedded Systems and Applications**

**Course Objectives:**

*The objective of this course is to give the students knowledge about Microcontroller & embedded systems. This course deals with the brief knowledge of Microcontroller MSP430, its architecture and assembly language programming for MSP430 microcontroller. The other objective of this course is know the application of embedded systems and interfacing with different devices like sensor, DAC, ADC, stepper motors, keyboard etc.*

**Unit I Basics of embedded computing-** Microprocessors, embedded design process, system description formalisms. Instruction sets- CISC and RISC; CPU fundamentals-programming I/Os, co-processors, supervisor mode, exceptions, memory management units and address translation, pipelining, super scalar execution, caching, CPU power consumption.

**Unit II Introduction of Microcontroller MSP 430:** RISC architecture, Instruction Sets and Addressing modes, I/O ports, counter and timers, interrupts and interrupt structure, Assembly Language Programming and Compiler-friendly features. Clock system, Memory subsystem. Key differentiating factors between different MSP 430 families.

**Unit III Interfacing I/O Interfacing,** understanding the multiplexing scheme of MSP 430 pins, LED, LCD, seven segment display, real time clock and Keyboard Interfacing. ADC, DAC, and Sensor Interfacing, Interfacing to External Memory, Interfacing to Stepper Motor.

**Unit IV Performance Issues of an Embedded System:** CPU performance–CPU Power Consumption, Analysis and Optimization of CPU Power Consumption, program execution time– Analysis, low-power modes (sleep modes), clock request feature, low power programming and interrupts.

**Unit V Applications of Embedded systems:** Energy meters, Smoke detectors, Data acquisition system, wired sensor network, and wireless sensor networks with Chipcon RF interface.

***Course Outcome (CO):***

At the end of this course students will have:

CO1 - To acquire knowledge about microcontrollers embedded processors and their applications.

CO2 - Foster ability to understand the internal architecture and interfacing of different peripheral devices with Microcontrollers.

CO3 - Foster ability to write the programs for microcontroller.

CO4 - Foster ability to understand the role of embedded systems in industry.

CO5 - Foster ability to understand the design concept of embedded systems.

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

<i>Cours e Outco me</i>	Program Outcome												Program Specific Outcome		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	P O9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
CO1	M	H								M				L	
CO2	M	H						H					L	H	L
CO3			H	M	L				L						M
CO4				H	H						L		H		
CO5						H	H					H			M

H = Highly Related; M = Medium L = Low

**Text Books**

1. Wolf, W. Computers as components- Principles of embedded computing system design. Academic Press (Indian edition available from Harcourt India Pvt. Ltd., 27M Block market, Greater Kailash II, New Delhi-110 048.).
2. Embedded System Design, A Unified Hardware/Software Introduction, Frank Vahid / Tony Givargis, 2006 reprint, John Wiley Student Edition.
3. An Embedded Software Primer, David .E. Simon, Fourth Impression 2007, Pearson Education.
4. John Davies, MSP430 Microcontroller Basics, Elsevier, 2008.
5. MSP430 Teaching CD-ROM, Texas Instruments, 2008 (Includes Power Point foils for Instructors.

### **Embedded System Laboratory**

#### **List of Experiments**

Programming and interfacing the MSP430 microcontroller

1. Introduction to general embedded system concepts. Participants will do some research on the net and familiarize themselves with the terminology associated with embedded systems.
2. General information regarding microcontrollers (microcontroller families, peripherals etc). Using mspdebug and msp430-gcc. This lesson introduces the tools you will use to program the msp430 microcontroller.
3. Writing our first msp430 program: use a GPIO pin to control an LED.
4. Understanding digital inputs. In this lesson, we learn to use a GPIO pin to read a mechanical switch.
5. Basics of Timer-A. Timers are very useful for a number of things like generating precise time delays, producing waveforms, counting events etc. In this lesson, we learn to use Timer-A of the msp430 microcontroller.
6. Understanding hardware interrupts.
7. Compiler optimizations - part 1. The compiler generates better quality code when you compile with optimizations enabled; but unless you understand what is really happening underneath, subtle bugs may bite you! In this lesson, we learn about the pitfalls associated with optimizations.
8. Analog to digital conversion - part 1. We learn to use the ADC on the MSP430 processor in this lesson.
9. Analog to digital conversion - part 2. An LED can be used as a light sensor! In this lesson, you will write a very interesting program which will use the msp430's ADC and an LED on the launchpad board to measure light intensity.
10. Running LED's - in this lesson, you will build a small running led display on a breadboard and interface it with the launchpad board!
11. Interfacing a seven segment display.
12. Implementing Pulse Width Modulation. PWM is a common technique used for applications like motor speed control.
13. Interfacing a potentiometer.
14. Programming the watchdog timer. The watchdog is an important part of the design of safety critical systems; in this lesson, you will learn how to program the msp430's watchdog timer.

#### ***Course Outcome (CO):***

At the end of this course students will have:

CO1 - To acquire knowledge about microcontrollers embedded processors and their applications.

CO2 - Foster ability to understand the internal architecture and interfacing of different peripheral devices with Microcontrollers.

CO3 - Foster ability to write the programs for microcontroller.

CO4 - Foster ability to understand the role of embedded systems in industry.

CO5 - Foster ability to understand the design concept of embedded systems.

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

<i>Cours e Outco me</i>	Program Outcome												Program Specific Outcome		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	P O9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
CO1	M	H								M				L	
CO2	M	H						H					L	H	L
CO3			H	M	L				L						M
CO4				H	H						L		H		
CO5						H	H					H			M

H = Highly Related; M = Medium L = Low

JECRC University  
**Faculty of Engineering & Technology**  
**M.Tech. in VLSI & Embedded System Semester II**  
**Contact Hours (L-T-P): 2 hrs per week**

### **System Modeling Lab Using Verilog/VHDL**

#### **Course Objective:**

*To develop hands on simulation tools that create a virtual environment which allows students to design and analyse any circuit. These skills will create a better understanding and help to implement this virtual design in the real world.*

#### **List of Experiments**

1. Modeling With Switch Primitives and Gate Primitives.
2. Modeling of 1-bit Full Adder.
3. Modeling of 32-bit CLA Adder.
4. Modeling of MUX.
5. Modeling of 32-bit ALU.
6. Modeling of Flip Flop and Latches.
7. Modeling of 8-bit Up and Down counter.
8. Modeling of 8-bit shift register with shift left and shift right mode of operation.
9. Modeling of ultimate CRC.
10. Modeling of First In First Out (FIFO).
11. Modeling of a serial adder with accumulator and verify using test bench.
12. Modeling of 4-bit multiplier.
13. Modeling of 1K RAM.
14. Modeling of simple UART.
15. Modeling of an 8-point FFT processor.

#### **Course Outcome (CO):**

At the end of this course students will have:

CO 1: Describe Verilog hardware description languages (HDL).

CO 2: Design Digital Circuits.

CO 3: Write behavioral models of digital circuits.

CO 4: Write Register Transfer Level (RTL) models of digital circuits.

CO 5: Verify behavioral and RTL models.

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

<i>Course Outcome</i>	Program Outcome												Program Specific Outcome		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
CO1	M	H								M				L	
CO2	M	H						H					L	H	L
CO3			H	M	L				L						M
CO4				H	H						L		H		
CO5						H	H					H			M

H = Highly Related; M = Medium L = Low

**Text Books**

1. *Samir Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis, 2nd Edition, Pearson.*
2. *Navabi. Introduction to VHDL. Mc Graw Hill, 2000*
3. *Bhaskar. VHDL Primer. Prentice Hall India, 2001*
4. *Navabi. Verilog digital systems. Mc Graw Hill, 2000*

**M.Tech. in VLSI & EMBEDDED SYSTEM Semester II**

	<b>Quantitative Techniques &amp; Computer Applications Lab</b>	<b>0-0-1</b>
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**Various Methods and Uses of Advance Excel Formulas:** Vlookup, Hlookup, Sumif, Sumifs, Sumproduct, Dsum, Countif, Countifs, If, Iferror, Iserror, Isna, Isnumber, Isnontext, Isblank, Istext, Getpivotdata, Dcount, Dcounta, Or, And, Search, Index, Match Etc

**Various Methods and Uses of IF Conditions:** When should use the "IF" Conditions?, Creation of Multiple IF Conditions in One Cell, Use the IF Conditions with the Other Advance Functions, How to use nested IF statements in Excel with AND, OR Functions

**ADVANCED EXCEL OPTIONS :** Various Methods of Filter and Advance Filter options, Creating and Updating Subtotals, Various Methods of Text to Column options, Uses of Data Grouping and Consolidation options, Uses of Goal Seek and Scenarios Manager, Various Method of Sorting Data, Creating, Formatting and Modifying Chart, Data Validation, Creating drop down lists using different data sources, Linking Workbooks and Uses of Edit Link options, Excel Options, Customizing the Quick Access Tool Bar, Formula Auditing features and Trace formula error

**Pivot Tables & Charts :** Various Methods and Options of Pivot Table, Using the Pivot Table Wizard, Changing the Pivot Table Layout, Subtotal and Grand total Options, Formatting, Grouping Items, Inserting Calculated Fields, Pivot Table Options, Calculation in Pivot Table, Display and Hide Data in Field, Select, Move & Clear Pivot Data, Creating and Modifying Pivot Chart

**Advance Use of Function:** Mixing Function to get Various MIS Outputs, Creating Data Table, Advance Data Validation, Using conditional formatting with Formulas and Function, Using Name Manager, Array Formulas

**Importing Data from External Sources: Macros,** What is a Macro?, Creating Excel Macro, Running Macros and Editing, Automating Tasks with Macro

**(A) SPSS Package**

**An Overview of SPSS :** Mouse and keyboard processing, frequently –used dialog boxes, Editing output, Printing results, Creating and editing a data file

**Managing Data:** Listing cases, replacing missing values, computing new variables, recording variables, exploring data ,selecting cases, sorting cases, merging files

**Graphs:** Creating and editing graphs and charts

**Frequencies:** Frequencies, bar charts, histograms, percentiles

**Descriptive Statistics:** measures of central tendency, variability, deviation from normality, size and stability, Cross Tabulation and chi-square analyses, The means Procedure

**Bivariate Correlation:** Bivariate Correlation, Partial, Correlations and the correlation matrix

**The T-test procedure:** Independent –samples, paired samples, and one sample tests

**The one way ANOVA procedure:** One way analysis of variance

**General Linear model:** Two –way analysis of variance

**General Linear model:** three –way analysis of variance and the influence of covariates, Simple Linear Regression, Multiple regression analysis, Multidimensional scaling, Factor analysis, Cluster analysis

***Course Outcome (CO):***

At the end of this course students will have:

CO1. Identify system components and utilize computer hardware and software.

CO2. Become proficient in using the features of word processing in Microsoft Word.

CO3. Become proficient in using spreadsheet software and be able to create technical and complex spreadsheets for data analyses using Microsoft Excel.

CO4. Develop effective and professional business presentations using Microsoft Power Point.

CO5. Use the internet to research information and enhance their documents.

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

<i>Course Outcome</i>	Program Outcome												Program Specific Outcome		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
CO1	M	H								M				L	
CO2	M	H						H					L	H	L
CO3			H	M	L				L						M
CO4				H	H						L		H		

CO5						H	H					H			M
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H = Highly Related; M = Medium L = Low

Text Book: Research Methodology – Methods & Techniques by C. R. Kothari, New age International Publisher

**Notes for Examiner / Paper Setter:**

1. 1<sup>st</sup> Question shall be of 16 marks and compulsory for all. It may consist of Multiple Choice Questions (MCQ) of one mark each and short answer questions of one or two marks.
2. One question of 14 marks shall be set from each Unit which may have parts including numericals. Paper setter may give internal choice, if required.
3. Students will be required to attempt all questions compulsorily.

**Testing and Testability of VLSI Circuits**

**Course Objectives:**

1. *Develop an understanding of test economics, failure mechanisms in VLSI circuits, and characterization of failures at various levels of circuit hierarchy.*
2. *Develop an understanding of reliability issues of VLSI circuits.*
3. *Utilize logic and fault simulation to develop test vector generation algorithms for combinational and sequential circuits.*
4. *Design testing methodologies for memory chips.*
5. *Utilize design for testability techniques including built-in self-test (BIST), scan design, and boundary scan.*
6. *Coordinate different testing tasks (combinational testing, sequential testing, memory testing, BIST, scan testing, etc.) so that a chip is tested as a whole entity.*
7. *Apply theoretical knowledge about algorithms to solve testing problems using a computer.*
8. *Use data structures and algorithms in C++ programs that are used to create testing software tools.*
9. *Use VHDL/Verilog to specify digital circuit structure and behavior and Altera FPGA development boards for testing.*
10. *Conduct literature survey on specific research topics, identify current challenges, and develop solutions.*

**Unit I Physical Faults and their modeling:** Stuck-at-Faults, Bridging Faults; Fault collapsing, Fault Simulation: Deductive, Parallel, and Concurrent Fault Simulation. Critical Path Tracing.

**Unit II ATPG for Combinational Circuits:** D-Algorithm, Boolean Differences, PODEM Random, Deterministic and Weighted Random Test Pattern Generation; Aliasing and its effect on Fault Coverage.

**Unit III PLA Testing,** Cross Point Fault Model and Test Generation. Memory Testing: Permanent, Intermittent and Pattern Sensitive Faults, Marching Tests: Delay Faults.

**Unit IV Unit II ATPG for Sequential Circuits:** Time Frame Expansion ; Controllability and Observability Scan Design, BILBO , Boundary Scan for Board Level Testing, BIST and

Totally self checking circuits.

**Unit V System Level Diagnosis & repair:** Introduction, Concept of Redundancy, Spatial Redundancy, Time Redundancy, Error Correction Codes. Reconfiguration Techniques: Yield Modeling, Reliability and effective area utilization.

**Course Outcome (CO):**

At the end of this course students will have:

- CO1: apply the concepts in testing which can help them design a better yield in IC design.
- CO2: tackle the problems associated with testing of semiconductor circuits at earlier design levels so as to significantly reduce the testing costs.
- CO3: analyse the various test generation methods for static & dynamic CMOS circuits.
- CO4: identify the design for testability methods for combinational & sequential CMOS circuits.
- CO5: recognize the BIST techniques for improving testability.

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

Course Outcome	Program Outcome												Program Specific Outcome		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
CO1	M	H								M				L	
CO2	M	H						H					L	H	L
CO3			H	M	L				L						M
CO4				H	H						L		H		
CO5						H	H					H			M

H = Highly Related; M = Medium L = Low

**Text Books**

1. Abramovici, M., Breuer, M. A. and Friedman, A. D. Digital systems testing and testable design. IEEE press (Indian edition available through Jayco Publishing house), 2001.
2. Bushnell and Agarwal, V. D. VLSI Testing. Kluwer.
3. Agarwal, V. D. and Seth, S. C. Test generation for VLSI chips. IEEE computer society press.
4. Hurst, S. L. VLSI testing: Digital and mixed analog/digital techniques. INSPEC/IEE, 1999.

### Image Processing in VLSI Design

#### **Course Objectives:**

1. Cover the basic theory and algorithms that are widely used in digital image processing.
2. Expose students to current technologies and issues that are specific to image processing.
3. Develop hands-on experience in using computers to process images.
4. Develop critical thinking about shortcomings of the state of the art in image processing.

**Unit I Introduction to Multirate systems and filter banks,** 2D systems and mathematical preliminaries, Digital Representation of Binary & Gray Scale and colour Images, Linear operations on images.

**Unit II Image sampling and quantization:** 2D Sampling on rectangular and nonrectangular sampling lattice, Aliasing, Lloyd-Max quantizer etc. Image Transforms: 2D Discrete Fourier transform, DCT, DST and Hadamard , Harr K-L Transforms & their applications to image processing.

**Unit III Image restoration:** Wiener filtering , smoothing splines and interpolation. Image Enhancement Techniques: Gray scale transformation, Histogram matching and equalization, Smoothing:-Noise Removal, Averaging, Median, Min/Max. Filtering, sharpening of Images using differentiation, the laplacian, High Emphasis filtering.

**Unit IV Image analysis:** Edge detection, Boundary Lines & Contours. Image representation by Stochastic models: ARMA models, 2D linear prediction. Image Segmentation & Thresholding: Multiband Thresholding, Thresholding from Textures, Selective histogram Technique.

**Unit V Image Compression:** Compression Techniques using K-L Transform, Block Truncation Compression. Error free Compression using Huffman coding & Huffman shift coding.

#### **Course Outcome (CO):**

At the end of this course students will have:

CO1 Understand the need for image transforms and their properties.

CO2 Choose appropriate technique for image enhancement both in spatial and frequency domains.

CO3 Identify causes for image degradation and apply restoration techniques.

CO4 Compare the image compression techniques in spatial and frequency domains.

CO5 Select feature extraction techniques for image analysis and recognition.

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

<i><b>Course Outcome</b></i>	Program Outcome												Program Specific Outcome		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
CO1	M	H								M				L	
CO2	M	H						H					L	H	L
CO3			H	M	L				L						M
CO4				H	H						L		H		
CO5						H	H					H			M

H = Highly Related; M = Medium L = Low

**Text Books**

1. Digital Signal Processing- Oppenheim A.V. & Schafer R.W. PHI.
2. Digital Signal Processing-by Mitra- (TATA McGraw Hill) Publications.
3. Digital Image Processing- by Gonzalez / Woods, (Pearson Education)
4. Digital Image Processing- by A.K. Jain
5. Digital Picture Processing- by Rosenfield & Kak

JECRC University

**Faculty of Engineering & Technology**

***M.Tech. in VLSI & Embedded System Semester III***

***Contact Hours (L-T-P) : 4-0-0***

**Hours: 48**

### **Wireless & Mobile Ad-Hoc Networks**

#### **Course Objectives:**

*This course is an advanced research-oriented course designed for graduate students with computer and wireless networks background. It will cover various topics relevant to a cutting-edge technology, namely, Wireless Ad Hoc Networks, which include Mobile Ad Hoc Networks (MANETs), Wireless Sensor Networks (WSNs) and Wireless Mesh Networks (WMNs). Through this course, students can learn the state of art of wireless ad hoc networks research, and enhance their potential to do research in this exciting area.*

**Unit I: TRANSMISSION CONCEPTS** Technical background - transmission fundamentals - communication networks –protocols and TCP/IP Suite - antennas and propagation signal - encoding techniques - spread spectrum coding and error control.

**Unit II: WIRELESS NETWORKING** Satellite communications- cellular transmission principles- cordless systems and wireless local loop mobile internet protocol and wireless access protocol.

**Unit III: WIRELESS LANs** Wireless local area network technology – institute of electrical and electronics engineering, 802 - 11 wireless local area network standard.

**Unit IV: CDMA STANDARDS** System architecture for code division multiple access - network and data link layers of code division multiple access – signaling applications in code division multiple access system - voice applications in code division multiple access system.

**Unit V: RF ENGINEERING AND FACILITIES** Wireless data - cellular communication fundamentals - global system for mobile communication architecture and interfaces – radio link features in global system for mobile communication - global system for mobile communication logical channels and frame structure - speech coding in global system for mobile communication.

#### ***Course Outcome (CO):***

At the end of this course students will have:

CO1: Understand the basic fundamentals of wireless communications

CO2: Aware about various wireless networks

CO3: Understand the depth technical aspects of WBAN,WPAN,WLAN and WMAN

CO4: Understand the concept of wireless ad-hoc network

CO5: To gain knowledge and experience in applying various computation methods and algorithms as a part of software development

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

<i>Course Outcome</i>	Program Outcome												Program Specific Outcome		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
CO1	M	H								M				L	
CO2	M	H						H					L	H	L
CO3			H	M	L				L						M
CO4				H	H						L		H		
CO5						H	H					H			M

H = Highly Related; M = Medium L = Low

**Text Book**

1. William Stallings, Wireless Communication and Networking, Pearson Education, Asia 2005.

**References**

1. Garg. V. K, Smolik. K, Applications of CDMA in Wireless/Personal Communications, Prentice Hall, 2004.
2. Garg V. K, Principles and Applications of GSM, Prentice Hall, 2002

## **EMBEDDED COMMUNICATION SOFTWARE DESIGN**

### **Course Objective:**

*The goal is adaptive wireless networking, self-organization techniques, and embedded system design with applications in ad hoc and sensor networks*

### **Unit I COMMUNICATION**

Open system interconnect reference model – communication devices – communication echo system – design consideration – host based communication – embedded communication system – operating system vs real time operating system.

### **Unit II SOFTWARE PARTITIONING**

Limitation of strict layering – tasks and modules – modules and task decomposition – layer2 switch – layer3 switch / routers – protocol implementation – management types – debugging protocols.

### **Unit III TABLES AND DATA STRUCTURES**

Partitioning of structures and tables – implementation – speeding up access – table resizing – table access routines – buffer and timer management – third party protocol libraries.

### **Unit IV MANAGEMENT SOFTWARE**

Device management – management schemes – router management – management of sub system architecture – device to manage configuration – system start up and configuration.

### **Unit V MULTI BOARD COMMUNICATION SOFTWARE DESIGN**

Multi board architecture – single control card and multiple lines card architecture – interface for multi board software – failures and fault – tolerance in multi board systems – hardware independent development – using a COTS board – development environment – test tools .

### **Course Outcome (CO):**

At the end of this course students will have:

CO1: Describe the differences between the general computing system and the embedded system, also recognize the classification of embedded systems..

CO2: Become aware of the architecture of the ATOM processor and its programming aspects (assembly Level)

CO3: Become aware of interrupts, hyper threading and software optimization.

CO4: Design real time embedded systems using the concepts of RTOS.

CO5: Analyze various examples of embedded systems based on ATOM processor.

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

<i>Cours e Outco me</i>	Program Outcome												Program Specific Outcome		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	P O9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
CO1	M	H								M				L	
CO2	M	H						H					L	H	L
CO3			H	M	L				L						M
CO4				H	H						L		H		
CO5						H	H					H			M

H = Highly Related; M = Medium L = Low

**Text Book**

1. Sridhar T, Designing Embedded Communication Software, CMP Books, 2004.
2. Greg Utas, Robust Communication Software John, Wiley and Sons, 2005.

**Low Power VLSI Design**

**Course objective:**

1. To give the student an understanding of the different design steps required to carry out a complete digital VLSI (Very-Large-Scale Integration) design in silicon.
2. To design chips used for battery-powered systems and high-performance circuits not exceeding power limits.

**Unit I Basics of MOS circuits:** MOS Transistor structure and device modelling, MOS Inverters, MOS Combinational Circuits - Different Logic Families. Sources of Power dissipation: Dynamic Power Dissipation, Short Circuit Power, Switching Power, Glitching Power, Static Power Dissipation, Degrees of Freedom

**Unit II Supply Voltage Scaling Approaches:** Device feature size scaling, Multi-Vdd Circuits, Architectural level approaches: Parallelism, Pipelining, Voltage scaling using high-level transformations, Dynamic voltage scaling, Power Management

**Unit III Switched Capacitance Minimization Approaches:** Hardware Software Tradeoff, Bus Encoding, Two's complement Vs Sign Magnitude, Architectural optimization, Clock Gating, Logic styles

**Unit IV Leakage Power minimization Approaches:** Variable-threshold-voltage CMOS (VTCMOS) approach, Multi-threshold-voltage CMOS (MTCMOS) approach, Power gating, Transistor stacking, Dual-Vt assignment approach (DTCMOS).

**Unit V Special Topics:** Adiabatic Switching Circuits, Battery-aware Synthesis, Variation tolerant design, CAD tools for low power synthesis.

**Course Outcome (CO):**

At the end of this course students will have:

- CO1 - Able to analyze the need for low power VLSI circuits
- CO2 - Able to understand dynamic and static power dissipation and factors affecting them
- CO3 - Able to Recognize Role of simulation possible at various levels of design
- CO4 - Able to define Relationship of probability while calculating power dissipation of circuits
- CO5 - Able to Apply Power reduction techniques possible at circuit ,logic level

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

<i>Cours e</i>	Program Outcome	Program Specific Outcome
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<b>Outcome</b>															
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
CO1	M	H								M				L	
CO2	M	H						H					L	H	L
CO3			H	M	L				L						M
CO4				H	H						L		H		
CO5						H	H					H			M

H = Highly Related; M = Medium L = Low

**Text Books**

1. Sung Mo Kang, Yusuf Leblebici, CMOS Digital Integrated Circuits, Tata Mcgrag Hill.
2. Neil H. E. Weste and K. Eshraghian, Principles of CMOS VLSI Design, 2nd Edition, Addison Wesley (Indian reprint).
3. A. Bellamour, and M. I. Elmasri, Low Power VLSI CMOS Circuit Design, Kluwer Academic Press, 1995.
4. Anantha P. Chandrakasan and Robert W. Brodersen, Low Power Digital CMOS Design, Kluwer Academic Publishers, 1995.
5. Kaushik Roy and Sharat C. Prasad, Low-Power CMOS VLSI Design, Wiley-Interscience, 2000.

### System Level Design & Modelling

#### **Course Objectives:**

1. *To understand what is a model, types of models, purpose of models.*
2. *To understand the need for quantification and understand the limits of quantification.*
3. *To transform loose facts into an insightful model, to be used as input for requirements discussions and system design and verification*
4. *To use scenario analysis as a means to cope with multiple alternative specifications and or designs.*
5. *To apply problem-driven light-weight simulations and understand their value and purpose in early design decisions.*
6. *To analyze dependability qualities, such as reliability, safety and security*
7. *To analyze the impact of changes; change and variation cases*
8. *To understand the value of rapid prototyping for: requirements, potential design issues, modeling inputs.*

**Unit I System level design, description languages** - SystemC, SDL, Spec Chart etc.  
Hardware-software,

**Unit II** codesign- partitioning, interface synthesis, case studies. Application specific processors,

**Unit III** Retargetable compilers, instruction set simulation and co-simulation.

**Unit IV** Architectural synthesis for DSP applications.

**Unit V Formal Verification of digital hardware systems-** BDD based approaches, functional equivalence, finite state automata,-automata, FSM verification. Model checking.

#### **Course Outcome (CO):**

At the end of this course students will have:

CO1.- Define basic concepts in modeling and simulation (M&S)

CO2. Classify various simulation models and give practical examples for each category

CO3. Construct a model for a given set of data and motivate its validity

CO4. Generate and test random number variates and apply them to develop simulation models

CO5. Analyze output data produced by a model and test validity of the model

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

<i>Cours e Outco me</i>	Program Outcome												Program Specific Outcome		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	P O9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
CO1	M	H								M				L	
CO2	M	H						H					L	H	L
CO3			H	M	L				L						M
CO4				H	H						L		H		
CO5						H	H					H			M

H = Highly Related; M = Medium L = Low

**Text Books**

1. Gajski, Gupta and Vahid, Specifications and design of Embedded systems
2. Topics on formal verification to be covered using topics from literature.

### **Robotics and Automation**

#### **Course Objectives:**

1. *Students will identify the definition and historical impact of technology.*
2. *Students can understand the impact of robotics and automation within global, economic, environmental and social needs.*

**Unit I Introduction:** Definition, Classification of Robots, Geometric classification and control classification.

**Unit II Robot Elements:** Drive systems, control systems, sensors, end effectors, Gripper actuators and gripper design.

**Unit III Robot Coordinate Systems and Manipulator Kinematics:** Robot co-ordinate system representation, transformations. Homogeneous transforms and its inverse, relating the robot to its world, manipulators kinematics, parameters of links and joints, kinematic chains, dynamics of kinematic chains, trajectory planning and control, advanced techniques of kinematics and dynamics of mechanical systems, parallel actuated and closed loop manipulators.

**Unit IV Robot Control:** Fundamental principles, classification, position, path and speed control systems, adaptive. Robot Programming: Level of robot programming, language based programming, task level programming, robot programming synthesis, robot programming for foundry,

**Unit V** Press work and heat treatment, welding, machine tools, material handling, warehousing assembly, etc., automatic storage and retrieval system, robot economics and safety, robot integration with CAD/ CAM/CIM, collision free motion planning.

#### **Course Outcome (CO):**

At the end of this course students will have:

- CO1 - Understand the basics of Robotics and Automation in the context using Robotic products
- CO2 - Understand the various skills needed to become an Robotic and Automation Expert
- CO3 - Understanding the process configurations and their realization of given robot.
- CO4 - Putting to effective use of a Robot through usage of software and programming
- CO5 - To develop an ability to use software tools for analysis and design of robotic systems.

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

<i>Course Outcome</i>	Program Outcome												Program Specific Outcome		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
CO1	M	H								M				L	
CO2	M	H						H					L	H	L
CO3			H	M	L				L						M
CO4				H	H						L		H		
CO5						H	H					H			M

H = Highly Related; M = Medium L = Low

**Text Books**

1. Robotic Technology(Vol I-V) Phillipe Collet Prentice Hall.
2. An Introduction to Robot Technology Coiffet and Chirooza Kogan Page.
3. Robotics for Enginners Y.Koren MGH
4. Robotics K.S. Fu, R.C. Gonzalez & CSG Lee MGH

**Advanced Artificial Neural Networks**

**Course Objectives:**

1. *Understand and explain strengths and weaknesses of the neural-network algorithms*
2. *Determine under which circumstances neural networks are useful in real application*
3. *Distinguish between supervised and unsupervised learning and explain the key principles of the corresponding algorithms*
4. *Efficiently and reliably implement the algorithms introduced in class on a computer, interpret the results of computer simulations*
5. *Describe principles of more general optimization algorithms.*
6. *Write well-structured technical reports in English presenting and explaining analytical calculations and numerical results*
7. *Communicate results and conclusions in a clear and logical fashion*

**Unit I Fundamentals:** Introduction & Motivation, Biological Neural Networks and simple models, The Artificial Neuron Model; Hopfield Nets; Energy Functions and Optimization; Neural Network Learning Rules: Hebbian Learning Rule, Perceptron Learning Rule, Delta Learning Rule Widrow-Hoff Rule, Correlation Learning Rule, Winner –Take-All Learning rule, Out Star Learning Rule, summary of Learning rules.

**Unit II Single layer perceptron classifiers:** Classification model, features and decision regions, discriminant functions, linear machine and minimum distance classification, nonparametric training concept training and classification using the discrete perceptron: algorithm and example, single layer continuous perceptron network for linearly separable classifications, multicategory

**Unit III Multilayer feed forward networks:** Linearly nonseparable pattern classification delta learning rule for multiperceptron layer. Generalized Delta Learning rule. Feed forward Recall and Error Back Propagation Training; Examples of Error Back-Propagation. Training errors: Learning Factors; Initial weights, Cumulative Weight Adjustment versus Incremental Updating, steepness of activation function, learning constant, momentum method, network architecture Versus Data Representation, Necessary number of Hidden Neurons. application of Back propagation Networks in pattern recognition & Image processing, Madaunes: Architecture & Algorithms.

**Unit IV Single Layer Feedback Network:** Basic concepts of dynamical systems, mathematical foundation of discrete-time hop field networks, mathematical foundation of Gradient-Type Hopfield networks, transient response of continuous time networks. example solution of optimization problems: summing networks with digital outputs, minimization of the traveling salesman tour length, solving simultaneous linear equations.

**Unit V Associative Memories I:** Basic concepts, linear associator basic concepts of recurrent auto

associative memory, retrieval algorithm, storage algorithm, storage algorithms performance considerations, performance concepts of recurrent auto associative memory, energy function reduction capacity of recurrent auto associative memory, memory convergence versus corruption, fixed point concept, modified memory convergence towards fixed points, advantages and limitations.

**Course Outcome (CO):**

At the end of this course students will have:

CO1-Ability to understand the fundamental and types of neural network models and various learning algorithms.

CO2- Ability to understand the layered models, their classification, algorithms and their application.

CO3-Ability to understand the feed forward and back propagation networks, their architecture and algorithms, application in speech recognition and image processing.

CO4-Ability to understand the concept of single layer feedback networks and application in solving various optimization problems

CO5-Ability to understand the concept associative memories and their various algorithms.

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

Course Outcome	Program Outcome												Program Specific Outcome		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
CO1	H		H		L			M			L			L	
CO2	L		L	L	M	L	M			H		L	L	H	L
CO3	H	M					L				L				M
CO4			L		H				L				H		
CO5	H	M					L				L				M

H = Highly Related; M = Medium L = Low

**Text Books**

1. J.M.Zurada: Introduction to Artificial Neural Systems, Jaico Publishers
2. Dr. B. Yagananarayana, Artificial Neural Networks, PHI, New Delhi.
3. Kishan Mehrotra, Chelkuri K. Mohan, Sanjay Ranka: Elements of Artificial Neural Networks, Penram International
4. Introduction Neural Networks Using MATLAB 6.0 - by S.N. Shivanandam, S. Sumati, S. N. Deepa,1/e, TMH, New Delhi.
5. Fundamental of Neural Networks – By Laurene Faus

**Synthesis of Digital Systems**

**Course Objective:**

*This course addresses design of digital systems at the RT-level, the VHDL language, synthesis, and FPGA technology. Focus is on writing efficient VHDL and on the relationship between VHDL constructs and the corresponding synthesized hardware implementations. A sequence of exercises supplements the lectures and provides hands on experience using VHDL and the associated CAD tools.*

**Unit I Design Technologies:** Motivation and perspectives Modelling Design languages and graphic formalisms, Role of CAD in digital system design, levels of design, modelling & description and support of languages, RTL, gate and system Level synthesis

**Unit II High-level synthesis:** Scheduling, Resource sharing, Data path and control synthesis

**Unit III Logic synthesis:** Algorithms and rule-based systems, Algebraic and Boolean methods, Timing issues,

**Unit IV Sequential synthesis and retiming:** Semi custom libraries & library mapping: Algorithms and rule-based systems, Structural and Boolean matching

**Unit V** Low power issues in high level synthesis and logic synthesis.

***Course Outcome (CO):***

At the end of this course students will have:

CO1- Synthesis of digital VLSI systems from register-transfer or higher level descriptions in hardware design languages.

CO2- . To understand the various design modeling and programming on different domains..

CO3- Be able to model complex digital systems at several level of abstractions; behavioral and structural, synthesis and rapid system prototyping.

CO4 - Be able to develop and simulate register-level models of hierarchical digital systems

CO5 - Be able to design and model complex digital system independently or in a team

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

<i>Course Outcome</i>	Program Outcome												Program Specific Outcome		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
CO1	M	H								M				L	
CO2	M	H						H					L	H	L
CO3			H	M	L				L						M
CO4				H	H						L		H		
CO5						H	H					H			M

H = Highly Related; M = Medium L = Low

**Text Books**

1. G. D. Micheli. Synthesis and optimization of digital systems.
2. Dutt, N. D. and Gajski, D. D. High level synthesis, Kluwer, 2000.
3. T. H. Cormen, C. E. Leiserson and R. L. Rivest, "Introduction to Algorithms," McGraw-Hill, 1990.
4. N. Deo, Graph Theory, PH India.

**VLSI System and Subsystem**

**Course Objectives:**

*To equip with an ability to apply knowledge of microelectronics devices & circuits.*

*2. An ability to design and conduct experiment related to VLSI*

*3. A knowledge and understanding of founding and fabrication processes*

*4. An ability to skillfully used design tools and learn different analog design based softwares.*

**Unit I** System specification using HDL : types of HDLs, Fundamentals of VHDL and Verilog, different type of modeling style.General VLSI Components

**Unit II** Arithmetic circuits in CMOS VLSI : Full adder, half adder, AOI logic, transmission gate logic, CPL logic, mirror technique, 4-bit parallel adder, carry look ahead adder, Manchester carry chain, high speed adder, multipliers, Array Multipliers.

**Unit III** Memories and Programmable logic: RAM, ROM, Row and column decoder, SRAM, SRAM Operation, DRAM, read, write and hold operation in DRAM, PLA, Gate array logic.

**Unit IV** System level physical design: interconnect, floorplanning, routing, input output circuits, power distribution and consumption

**Unit V** VLSI clocking and system design: Clock generation and distribution, clock stabilization and generation, Timing circle and clock skew, clock routing.Reliability and testing of VLSI circuits

***Course Outcome (CO):***

At the end of this course students will have:

CO1-Ability to understand MOSFET and their fabrication.

CO2- Ability to understand any combinational circuit analysis using MOSFET

CO3-Ability to understand & analyse sequential MOS circuits

CO4-Ability to draw layout of any circuit.

CO5-Ability to understand hardware description language.

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM  
OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

<i>Course Outcome</i>	Program Outcome												Program Specific Outcome		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
CO1	H		H		L			M			L			H	
CO2	L		L	H	M	L				H		L	L		M
CO3	L	M		H			L				L				H
CO4			L		H		H						H		
CO5	H	M					H							M	

H = Highly Related; M = Medium L = Low

**Text Books:**

1. *VLSI Circuits and Systems by John P. Uyemura.*

### ADVANCED MICROPROCESSORS

#### **Course Objectives:**

*The objective of this course is to give the students the ability to design, build and test a microprocessor-based controller system. Students will learn how a microprocessor works, and programming in assembly language. Other objectives of this course are to present fundamental concept and their architecture, to make students aware of techniques of interfacing between processor and peripheral devices.*

**UNIT I : 16/ 32 BIT MICROPROCESSOR** Organization of 8086/ 8088 microprocessors - Minimum maximum mode - Pipeline Architecture - Registers - Addressing modes - Memory Registration - Memory Segmentation - Instruction set of 8086/ 8088 - Bus structure and timing - exception handling, PIC Microcontroller.

#### **UNIT II: ASSEMBLY LANGUAGE PROGRAMMING**

Assembly language programming of 8086 microprocessor - Data transfer instruction - Arithmetic instruction - Branch instructions - Loop instructions - NOP and HALT instructions - Flag manipulation instructions - Logical instructions - Shift and rotate instructions - linking and relocation - stacks procedure - Interrupts and interrupt routines - Macros - Byte and string manipulations.

#### **UNIT III: DIGITAL INTERFACING**

Programming Parallel ports - Handshake input/output - interfacing a microprocessor to a keyboard, interfacing to alphanumeric displays, interfacing a microcomputer to high power devices, Optical motor shaft encoders - Sensors and Transducers - D/A converter operations, interfacing & applications- A/D converter Specifications, types & interfacing, A 8086 based process control system.

**UNIT IV: MULTIPROCESSOR CONFIGURATIONS** Queue status and lock facilities - 8086 / 8088 based multiprocessing system, 8087 numeric data processor, 8089 I/O processor, Motorola and Texas Instruments.

**UNIT V: SOFTWARE AND EXPANSION METHOD** Queues- Tables and strings - Program organization - State machines - timing consideration- UART ports - Input / Output serial ports programmable controllers - Fuse programmable controllers.

#### **Course Outcome (CO):**

At the end of this course students will have:

CO1. Write programs to run on 8086 microprocessor based systems.

CO2. Design system using memory chips and peripheral chips for 16 bit 8086 microprocessor.

CO3. Understand and devise techniques for faster execution of instructions, improve speed of operations and enhance performance of microprocessors.

CO4. Distinguish between RISC and CISC processors.

CO5. Understand multi core processor and its advantages.

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

<i>Cours e Outco me</i>	Program Outcome												Program Specific Outcome		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	P O9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
CO1	M	H								M				L	
CO2	M	H						H					L	H	L
CO3			H	M	L				L						M
CO4				H	H						L		H		
CO5						H	H					H			M

H = Highly Related; M = Medium L = Low

**Text Books**

- LIU.Y and GIBSON. G. A., “Microcomputer systems : The 8086/ 8088 family : Architecture, Programming and design”, Prentice Hall of India Pvt. Ltd, M.D. (1979)
- HALL.D.V, “Microprocessor and Interfacing : Programming and hardware”, McGraw Hill Book Company, New York, (1988)

JECRC University

Faculty of Engineering & Technology

*M.Tech. in VLSI & Embedded System Semester III*

*Contact Hours (L-T-P): 4-0-0*

**Hours: 48**

**Architecture of Digital Signal Processors**

**Course Objectives:**

*The objective of this course is to give the students knowledge of designing digital signals processors, the architecture of DSP processors and computational characteristics of DSP algorithms. This course also includes the knowledge of Architecture of Texas Instruments fixed-point and floating-point DSPs like TMS320C5x /C54x/C3x, Lucent Technologies' DSP 16000 VLIW processors and recent processors.*

**Unit I:** Computational characteristics of DSP algorithms and applications; their influence on defining a generic instruction-set architecture for DSPs.

**Unit II:** Architectural requirement of DSPs: high throughput, low cost, low power, small code size, embedded applications. Techniques for enhancing computational throughput: parallelism and pipelining.

**Unit III:** Data-path of DSPs: multiple on-chip memories and buses, dedicated address generator units, specialized processing units (hardware multiplier, ALU, shifter) and on-chip peripherals for communication and control. Control-unit of DSPs: pipelined instruction execution, specialized hardware for zero-overhead looping, interrupts.

**Unit IV:** Architecture of Texas Instruments fixed-point and floating-point DSPs: brief description of TMS320C5x /C54x/C3x and recent DSPs; Programmer's model. Architecture of Analog Devices fixed-point and floating-point DSPs: brief description of ADSP 218x / 2106x and recent DSPs; Programmer's model;

**Unit V:** Advanced DSPs: TI's TMS 320C6x, ADI's Tiger-SHARC, Lucent Technologies' DSP 16000 VLIW processors. Applications: a few case studies of application of DSPs in communication and multimedia.

***Course Outcome (CO):***

At the end of this course students will have:

CO1- Recognize the fundamentals of fixed and floating point architectures of various DSPs.

CO2- Learn the architecture details and instruction sets of fixed and floating point DSP

CO3- Infer about the control instructions, interrupts, and pipeline operations.

CO4- Analyze and learn to implement the signal processing algorithms in DSPs

CO5- Learn the DSP programming tools and use them for applications & design and implement signal processing modules in DSPs

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

Course Outcome	Program Outcome												Program Specific Outcome		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
CO1	H		H		L			M			L			L	
CO2	L		L	L	M	L				H		L	L	H	L
CO3	H	M					L				L				M
CO4			L		H								H		
CO5	H	M					L								M

H = Highly Related; M = Medium L = Low

**Texts/References:**

1. P. Pirsch: *Architectures for Digital Signal Processing*; John Wiley.
2. R. J. Higgins: *Digital Signal Processing in VLSI*; Prentice-Hall.
3. *Texas Instruments TMS320C5x, C54x and C6x Users Manuals*.
4. *Analog Devices ADSP 2100-family and 2106x-family Users Manuals*.
5. K. Parhi: *VLSI Digital Signal Processing Systems*; John Wiley.
6. K. Parhi and T. Nishitani: *Digital Signal Processing for Multimedia Systems*; Marcel Dekker.
7. *IEEE Signal Processing Magazine*: Oct 88, Jan 89, July 97, Jan 98, March 98 and March 2000.

## **EMBEDDED HARDWARE**

### **Course Objective:**

*To teach students all aspects of the design and development of an embedded system, including hardware and embedded software development. The course utilizes and applies the skills and knowledge students have gained throughout their prior undergraduate curriculum. Individual (rather than team) lab assignments ensure that each student is able to apply engineering theory to real world designs.*

### **Unit I: EMBEDDED HARDWARE**

Concept – Memory, DMA, Block diagram of embedded computer, Register, Stack, Firmware, Schematic – component with net – Power sources – Regulator – LM78xx Regulator, Max602/603 Regulator, Max1615 Regulator, Max724 Regulator - battery, low power design.

### **Unit II: BUILDING HARDWARE**

Tools – Development kit – measurement tools – Construction tools – Soldering – soldering surface mount component using rework station – quick construction – Bread boarding - wire wrapping - PCB – JTAG.

### **Unit III: ADDING PERIPHERALS AND SERIAL PORT**

Adding peripherals using SPI, Serial peripheral interface - adding peripherals using I2C – overview of I2C - adding real time clock with I2C – adding small display with I2C – Serial port – UART – RS232 – RS422 – RS485 – IrDA – USB – device classes – device packet – physical interface – Implementing USB interface.

### **Unit IV: ANALOG AND DIGITAL CONVERSION**

Amplifier – ADC – Interfacing an external ADC – Temperature sensor – Light sensor – Accelerometer – Pressure sensor – Magnetic field sensor – DAC – PWM – Motor control – Switching big loads – MC33298.

### **Unit V: EMBEDDED APPLICATIONS**

Motor control with PIC – PIC based environment data logger – AVR based data logger – simple 68HC11 based computer – MAXQ overview – Simple 68000 based computer – DSP 56805 based computer.

### **Course Outcome (CO):**

At the end of this course students will have:

CO1 - To acquire knowledge about microcontrollers embedded processors and their applications.

CO2 - Foster ability to understand the internal architecture and interfacing of different peripheral devices with Microcontrollers.

CO3 - Foster ability to write the programs for microcontroller.

CO4 - Foster ability to understand the role of embedded systems in industry.

CO5 - Foster ability to understand the design concept of embedded systems.

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

<i>Course Outcome</i>	Program Outcome												Program Specific Outcome		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
CO1			L		L			M			L			H	
CO2	M		H	L	M	L				H		L	M	H	L
CO3	H	M					L				L				M
CO4			L		H								H		
CO5	H	M					L								M

H = Highly Related; M = Medium L = Low

**Text Books**

1. John Catsoulis, Designing Embedded Hardware, O'Reilly Publisher, 2<sup>nd</sup> Edition, 2005.
2. Jean J. Labrosse, Embedded Systems Building Blocks: Complete and Ready-To-Use Modules in C, CMP Books, 2005.

**References**

1. Ball S. R, Embedded microprocessor Systems – Real World Design, Prentice Hall, 2001.
2. Daniel W. Lewis, Fundamentals of Embedded Software where C and Assembly meet, PHI, 2002

JECRC University

Faculty of Engineering & Technology

*M.Tech. in VLSI & Embedded System Semester III*

*Contact Hours (L-T-P): 4-0-0*

**Hours: 48**

### **DATA COMPRESSION TECHNIQUES**

#### **Course Objectives:**

1. *Understand the two major compression techniques, their merits and demerits.*
2. *Discuss important issues in data compression.*
3. *Estimate the effect and efficiency of a data compression algorithm.*
4. *Use lossless and lossy applications to compress data/multimedia.*
5. *Learn how to design and implement compression algorithms.*

#### **Unit I: COMPRESSION FEATURES**

Special features of multimedia – graphics and image data representations – fundamental concepts in video and digital audio – storage requirements for multimedia applications - need for compression - taxonomy of compression techniques – overview of source coding, source models, scalar and vector quantization theory – evaluation techniques – error analysis and methodologies.

#### **Unit II TEXT COMPRESSION**

Compaction techniques – huffmann coding, adaptive huffmann coding, arithmetic coding, shannon-fano coding, dictionary techniques, Lempel-Ziv-Welch family algorithms .

#### **Unit III: AUDIO COMPRESSION**

Audio compression techniques-  $\mu$ - law and a- law companding. frequency domain and filtering – basic sub-band coding – application to speech coding – G.722 – Application to audio coding – moving picture expert group audio, progressive encoding for audio – silence compression, speech compression techniques – format and CELP Vocoders.

#### **Unit IV: IMAGE COMPRESSION**

Predictive techniques – delta modulation, pulse code modulation, differential pulse code modulation - optimal predictors and optimal quantization – contour based compression – transform coding – joint photographic expert group standard – sub-band coding algorithms - design of filter banks – wavelet based compression - implementation using filters – embedded zerotree wavelet, set partitioning in hierarchical trees coders – joint photographic expert group 2000 standards - JBIG, JBIG2 standards.

#### **Unit V: VIDEO COMPRESSION**

Video compression techniques and standards – moving picture expert group video coding I moving picture expert group – 1 and 2 – moving picture expert group video coding II – moving picture expert group – 4 and 7 – motion estimation and compensation techniques– H.261 Standard, digital visual interface technology – production level video performance – digital visual interface real time compression, packet video.

#### ***Course Outcome (CO):***

At the end of this course students will have:

CO1 - Explain the evolution and fundamental concepts of Data Compression and Coding techniques.

CO2 - Analyze the operation of a range of commonly used Coding and Compression techniques

CO3 - Identify the basic software and hardware tools used for data compression.

CO4 - Identify what new trends and what new possibilities of data compression are available

CO5 - student will be able to define compression; understand compression as an example of representation.

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

<i><b>Course Outcome</b></i>	<b>Program Outcome</b>												<b>Program Specific Outcome</b>		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
CO1	M	H								M				L	
CO2	M	H						H					L	H	L
CO3			H	M	L				L						M
CO4				H	H						L		H		
CO5						H	H					H			M

H = Highly Related; M = Medium L = Low

**Text Books**

1. Peter Symes, Digital Video Compression, McGraw Hill Pub., 2004.
2. Mark S. Drew, Ze-Nian Li, Fundamentals of Multimedia, PHI, 1<sup>st</sup> Edition, 2003.
3. Khalid Sayood, Introduction to Data Compression, Morgan Kauffman Harcourt India, 2<sup>nd</sup> Edition, 2000.
4. David Salomon, Data Compression – The Complete Reference, Springer Verlag New York Inc., 2<sup>nd</sup> Edition, 2001.
5. Yun Q.Shi, Huifang Sun, Image and Video Compression for Multimedia Engineering - Fundamentals, Algorithms & Standards, CRC press, 2003.

JECRC University

Faculty of Engineering & Technology

*M.Tech. in VLSI & Embedded System Semester III*

*Contact Hours (L-T-P): 4-0-0*

**Hours: 48**

### **ADVANCED DIGITAL SIGNAL PROCESSING**

#### **Course Objective:**

*The goal of advanced digital signal processing course is to provide a comprehensive coverage of signal processing methods and tools, including leading algorithms for various applications.*

#### **Unit I: DIGITAL SIGNAL PROCESSING**

Digital signal processing - sampling of analog signals, selection of sample frequency, signal-processing systems, frequency response, transfer functions, signal flow graphs, filter structures, adaptive digital signal processing algorithms, discrete fourier transform - the discrete fourier transform, fast fourier transform - fast fourier transform algorithm, image coding, discrete cosine transforms.

#### **Unit II: DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS**

Finite impulse response filters – finite impulse response filter structures, finite impulse response chips, infinite impulse response filters, specifications of infinite impulse response filters, mapping of analog transfer functions, mapping of analog filter structures.

#### **Unit III: MULTIRATE DSP**

Decimation by a factor D, interpolation by a factor i, filter design and implementation for sampling rate conversion, multistage implementation of sampling rate conversion - sampling rate conversion by an arbitrary factor – applications of multirate signal processing digital filter banks - quadrature mirror filter bank.

#### **Unit IV: DSP PROCESSORS AND DSP APPLICATIONS**

General purpose Digital Signal Processors: Texas Instruments TMS320 family Motorola DSP 56333 family – analog devices ADSP 2100 family – Instruction set of TMS320C50 – simple programs. FFT Spectrum Analyser – musical sound processing. Power System Applications, Image Processing Applications.

#### **Unit V: ARITHMETIC UNITS AND INTEGRATED CIRCUIT DESIGN**

Conventional number system, redundant number system, residue number system - bit-parallel and bit-serial arithmetic, basic shift accumulator, reducing the memory size, complex multipliers, improved shift - accumulator - layout of very large scale integrated circuits, fast fourier transform processor, discrete cosine transform processor and interpolator as case studies.

#### ***Course Outcome (CO):***

At the end of this course students will have:

CO1- Recognize the fundamentals of fixed and floating point architectures of various DSPs.

CO2- Learn the architecture details and instruction sets of fixed and floating point DSP

CO3- Infer about the control instructions, interrupts, and pipeline operations.

CO4- Analyze and learn to implement the signal processing algorithms in DSPs

CO5- Learn the DSP programming tools and use them for applications & design and implement signal processing modules in DSPs

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

<i>Course Outcome</i>	Program Outcome												Program Specific Outcome		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
CO1	H		H		L			M			L			L	
CO2	L		L	L	M	L				H		L	L	H	L
CO3	H	M					L				L				M
CO4			L		H								H		
CO5	H	M					L								M

H = Highly Related; M = Medium L = Low

**Text Book**

1. Monson H. Hayes, Statistical Digital Signal Processing and modeling, John Wiley and sons, 2003.
2. Sajit K. Mitra, ‘Digital Signal Processing – A Computer Based Approach’, Tata McGraw Hill Publishing Company Ltd., New Delhi, 1998
3. John G. Proakis and Dimitris G. Manolakis, ‘Digital Signal Processing, Algorithms and Applications’. PHI, New Delhi, 1995
4. Lars Wanhammer, DSP Integrated Circuits, Academic press, New York, 2002.
5. Oppenheim. A. V, Discrete-time Signal Processing Pearson education, 2000.
6. Emmanuel C. Ifeakor, Barrie W. Jervis, Digital signal processing – A practical approach, 2<sup>nd</sup> edition, Pearson edition, Asia.

### Advanced Digital System Design

#### Course Objectives:

1. To introduce methods to analyze and design synchronous and asynchronous sequential circuits
2. To introduce variable entered maps and techniques to simplify the Boolean expressions using these maps.
3. To explain the design procedures for developing complex system controllers using digital ICs.
4. Become familiar with digital system concept and designing steps/methods.
5. Understand and design sequential digital circuits with various aspects.
6. Learn advanced methods for digital system design.
7. Understand designing using VHDL in digital systems.
8. Study various case studies in digital system design

**Unit I: Sequential circuit design:** Analysis of Clocked Synchronous Sequential Networks (CSSN) modelling of CSSN, state stable assignment and reduction, Design of CSSN, design of Iterative Circuits, ASM Chart , ASM Realization, Design of Arithmetic circuits for Fast adder, array Multiplier.

**Unit II: Asynchronous sequential circuit design:** Analysis of Asynchronous Sequential Circuit (ASC) Flow Table Reduction, Races in ASC, state assignment problem and the transition table design of ASC, static and dynamic hazards, essential hazards, data synchronizers, designing vending machine controller, mixed operating mode asynchronous circuits.

**Unit III: Fault diagnosis and testability algorithms:** fault table ,method, path sensitization method, boolean difference method, Kohavi algorithm, tolerance techniques, The Compact Algorithm, practical PLAs, fault in PLA, test generation, masking cycle , DFT Schemes, built-in self Test.

**Unit IV: Synchronous design using programmable devices:** Programming techniques, Re-programmable devices architecture, function blocks, I/O blocks, interconnects, realize combinational, arithmetic, Sequential circuit with programmable array logic; architecture and application of Field Programmable Logic Array.

**Unit V: New generation programmable logic devices:** Foldback architecture with GAL, EPLD, EPLA, PEEL, PML; PROM – Realization State machine using PLD , FPGA , Xilinx

FPGA , Xilinx 2000 , Xilinx 3000.

**Course Outcome (CO):**

At the end of this course students will have:

- CO1 - understand the functionality of digital systems,
- CO2 - analyze and synthesize digital modules and circuits for a wide application range,
- CO3 - design and implement hardware digital systems incorporating memory modul
- CO4 - model, simulate and implement digital circuits using hardware description languages and CAD tools,
- CO5 - Interpret the specifications of programmable reconfigurable devices and select the appropriate for the application in hand.

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

Course Outcome	Program Outcome												Program Specific Outcome		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
CO1	M	H								M				L	
CO2	M	H						H					L	H	L
CO3			H	M	L				L						M
CO4				H	H						L		H		
CO5						H	H					H			M

H = Highly Related; M = Medium L = Low

**Text Books:**

1. Donald G. Givone, “Digital principles and Design”, Tata McGraw Hill 2002.
2. Stephen Brown and Zvonk Vranesic, “Fundamentals of Digital Logic with VHDL Deisgn”, Tata McGraw Hill, 2002.
3. Mark Zwolinski, “Digital System Design with VHDL”, Pearson Education, 2004.
4. Parag K Lala, “Digital System design using PLD”, BS Publications, 2003. 5. John M Yarbrough, “Digital Logic applications and Design”, Thomson Learning, 2001.
5. Nripendra N Biswas, “Logic Design Theory”, Prentice Hall of India, 2001. 7. Charles H. Roth Jr., “Fundamentals of Logic design”, Thomson Learning, 2004.

**SOFT COMPUTING**

**Course Objectives:**

1. *Soft computing refers to principle components like fuzzy logic, neural networks and genetic algorithm, which have their roots in Artificial Intelligence.*
2. *Healthy integration of all these techniques has resulted in extending the capabilities of the technologies to more effective and efficient problem solving methodologies*
3. *Identify and describe soft computing techniques and their roles in building intelligent machines.*
4. *Recognize the feasibility of applying a soft computing methodology for a particular problem.*
5. *Apply logic and reasoning to handle uncertainty and solve engineering problems.*
6. *Apply genetic algorithms to combinatorial optimization problems.*
7. *Apply neural networks to pattern classification and regression problems effectively use existing software tools to solve real problems using a soft computing approach.*
8. *Evaluate and compare solutions by various soft computing approaches for a given problem.*

**Unit I: ARTIFICIAL INTELLIGENCE (AI)**

Intelligent search – Predicate Calculus – Learning Systems - Knowledge Representation and Reasoning – Semantic Networks – Frames - Knowledge Acquisition - Expert Systems - Intelligent Control.

**Unit II: ARTIFICIAL NEURAL NETWORKS (ANN)** Biological Neural Networks - Artificial Neural Networks - Topology of ANN – Learning rules – Supervised, Unsupervised, and Reinforcement Learning – Single Layer and Multilayer Perceptrons - Feed forward neural networks-The Back-propagation Training Algorithm - Binary and Continuous Hopfield Network - Associative Memory – Self Organizing Maps.

**Unit III: FUZZY SYSTEMS:** Classical Set – Fuzzy Set – Linguistic Variables Membership Functions - Fuzzy relations – Fuzzy rules and Reasoning – Fuzzy Inference Systems-Defuzzification methods – Mamdani, Sugeno and Tsukamoto Fuzzy models – Fuzzy Decision Making – Fuzzy logic control.

**Unit IV: GENETIC ALGORITHMS (GA):** Survival of Fittest – GA Terminologies Working Principle of Binary GA – Genetic Operators – Reproduction, Cross over and Mutation – Similarities and Differences with traditional methods – Schema and Schemata – GA theorem – Real Coded GA - Advantages and Limitations of GA – Applications.

**Unit V: CASE STUDIES/APPLICATIONS:** Case studies in neural networks - Applications of fuzzy logic control - Hybrid system- Neuro fuzzy system-ANFIS applications.

**Course Outcome (CO):**

At the end of this course students will have:

CO1 - To know about the basics of soft computing techniques and also their use in some real life situations.

CO2 - To solve the problems using neural networks techniques.

CO3 - To find the solution using different fuzzy logic techniques

CO4 - To use the genetic algorithms for different modelling

CO5 - To integrate the various soft computing techniques

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

Course Outcome	Program Outcome												Program Specific Outcome		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
CO1	M	H								M				L	
CO2	M	H						H					L	H	L
CO3			H	M	L				L						M
CO4				H	H						L		H		
CO5						H	H					H			M

H = Highly Related; M = Medium L = Low

**Text Book:**

1. J.S.R. Jang., et al., “Neuro-Fuzzy and Soft Computing: A Computational Approach to Learning and Machine Intelligence”, PHI, 2010.
2. Amit Konar, “Artificial Intelligence and Soft Computing: Behavioral and Cognitive modeling of the Human Brain”, CRC Press, 2008.
3. Simon Haykin, “Neural Networks and Learning Machines”, 3<sup>rd</sup> Edition, Pearson, 2009.
4. Timothy J. Ross, “Fuzzy Logic with Engineering Applications”, 3<sup>rd</sup> Edition, Wiley, 2010.
5. Kalyanmoy Deb, “Multi-Objective Optimization Using Evolutionary Algorithms”, 3<sup>rd</sup> Edition, Wiley, 2010.
6. David E. Goldberg, “Genetic Algorithms in Search, Optimization and Machine Learning”, Pearson, 2009.
7. N.P.Padhy, “Artificial Intelligence and Intelligent Systems”, Oxford University Press, 2008.

JECRC University

Faculty of Engineering & Technology

*M.Tech. in VLSI & Embedded System Semester III*

*Contact Hours (L-T-P): 3-0-0*

Hours: 36

### **ADVANCED COMPUTER ARCHITECTURE**

#### **Course Objectives:**

1. *Understand the advanced concept of computer architecture.*
2. *Understand the concept of complete system consisting of asynchronous interactions between concurrently executing hardware components & device driver software in order to illustrate the behaviour of a computer system as a whole.*

#### **Unit I: UNIPROCESSOR AND PARALLEL COMPUTER STRUCTURE**

Basic Uniprocessor Architecture - Parallel processing Mechanisms- Balancing of Subsystem band width- Parallel Computer structure- Architectural classifications- Parallel processing applications.

#### **Unit II: PARALLEL COMPUTER MODELS AND PERFORMANCE**

Parallel Computer Models - Multi processing and Multi computers- Multi vector and SIMD Computers - PRAM and VLSI Models. Principles of Scalable Performance - Performance Metrics and measures- Speedup. Performance laws- Scalability Analysis and Approaches.

**Unit III: MEMORY** Processors and memory Hierarchy- Advanced Processor Technology-Super scalar and Vector processors- Memory hierarchy technology- Virtual memory Technology. Bus- cache- and shared memory- Backplane Bus Structure- Cache memory organizations- Shared memory organizations.

**Unit IV: DESIGN AND PIPELINING:** Pipelining and super scalar techniques- Linear pipe line Processors- Non linear pipeline processors- Instruction pipeline design- Arithmetic pipeline design- Super scalar and super pipeline design.

**Unit V: MULTIPROCESSOR AND COMPOUND VECTOR PROCESSING:** Multi processors and Multi computers- Multi processor system interconnects- Cache coherence and Synchronization Mechanism- Message passing mechanisms. Multi vector and SIMD Computers- Vector processing principles- Compound vector processing- SIMD Computer organizations.

#### **Course Outcome (CO):**

1. Master the binary and hexadecimal number systems including computer arithmetic,
2. Be familiar with the history and development of modern computers,
3. Be familiar with the Von Neumann architecture,
4. Be familiar with the functional units of the processor such as the register file and arithmetic-logical unit,

5. Be familiar with the basics of systems topics: single-cycle (MIPS), multi-cycle (MIPS), parallel, pipelined, superscalar, and RISC/CISC architectures.

<i>Course Outcome</i>	Program Outcome												Program Specific Outcome		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
CO1	H		H		L			M			L			L	
CO2	L		L	L	M	L				H		L	L	H	L
CO3	H	M					L		M		L				M
CO4			L		H					L			H		
CO5	H	M					L				L	L			M

H = Highly Related; M = Medium L = Low

**Text Books**

1. A Kai Hwang, Advanced Computer Architecture - Kai Hwang, McGraw-Hill, Inc - 1987
2. Kai Hwang and Faye A. Briggs Computer Architecture and Parallel Processing, McGraw - Hill(1989.)
3. Rafiquzzaman, and Chandra -Modern computer Architecture-West Publishing Company, 1989
4. Morris Mano -Computer system Organization- Prentice Hall of India, 3rd ed,(1993.)
5. Andrew s. Tannenbaum -Computer Organization -Prentice (1991)

### **DESIGN OF DIGITAL CONTROL SYSTEM**

#### **Course Objectives:**

1. Knowledge about principles and techniques of A/D and D/A conversions and basics of Z-transforms.
2. Knowledge in stability analysis of digital control systems.
3. Knowledge about the design of digital control system for different engineering model.

#### **UNIT I - Sampling And Reconstruction- Transform Analysis Of Sample Data Systems**

Effects of sampling- Sampled data control systems- A/D & D/A conversion- Fourier transform- z-transform- Pulse transform function- Stability analysis- Time and frequency response.

#### **UNIT II - DESIGN USING TRANSFORM AND STATE SPACE TECHNIQUES**

Digital PID controller- Multivariable controller- Discrete time state equation- Cayley-Hamilton theorem- Concepts of controllability and observability- Lyapunov stability analysis.

#### **UNIT III - SELF TUNING CONTROL**

Introduction- Principle of least square- Recursive least square algorithm- minimum- Variable prediction- Minimum-Variance control- Self-tuning regulators.

#### **UNIT IV - MICROPROCESSOR BASED CONTROL & ASYNCHRONOUS SERIAL COMMUNICATION**

General description of microcontrollers- Digital quantization- Position control- Process model- Control algorithm- hardware mechanization- System software. Asynchronous serial communication - RS 232 - RS 485 - Sending and receiving data - Serial ports on PC - Low level PC serial I/O module - Buffered serial I/O.

#### **UNIT V- STEPPING MOTORS AND THEIR INTERFACING TO MICROPROCESSOR**

Introduction- Constructional & operational features of stepping motors-important parameters of stepping motors-Stepping motor drive circuits-Interfacing to microprocessor.

#### **Course Outcome (CO):**

At the end of this course students will have:

- CO1. Understand control system design techniques, their limitations and benefits.  
CO2. Become familiar with issues faced in sampling, digital data and discrete time systems.

CO3. Gain experience in designing digital controllers either by emulating continuous time compensators or by direct digital design using the Root Locus and Frequency Response methods. (EAC c)

CO4. Be given a brief introduction to digital filter design.

CO5. The students should be able to use ordinary differential equations and Laplace transformation to model physical systems

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

<i>Course Outcome</i>	Program Outcome												Program Specific Outcome		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
CO1	M	H								M				L	
CO2	M	H						H					L	H	L
CO3			H	M	L				L						M
CO4				H	H						L		H		
CO5						H	H					H			M

H = Highly Related; M = Medium L = Low

**Text Books**

1. GOPAL M , “ Digital Control Engineering “, New age international .1996
2. Digital Control Systems: B.C.Kuo.(Holt - saunders Japan Ltd.)-1991

**References**

1. K. Ogata , “Discrete Time control systems”, PHI 1987
2. Forsytheand W.Goodall R.N. “Digital Control” Mc Millan, 1991
3. Design control system design : Samita, Stubberud Hostelier(Hercourt brace college publisher)- 1988.

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*Contact Hours (L-T-P): 3-0-0*

Hours: 36

### **CRYPTOGRAPHY AND NETWORK SECURITY**

#### **Course Objectives:**

1. *To provide an introduction to the fundamental principles of cryptography and its applications on the network security domain.*
2. *To study various approaches to encryption techniques, strengths of traffic confidentiality, message authentication codes.*
3. *To illustrate how network security and management mechanism employ cryptography to prevent, detect, and mitigate security threats against the network.*

#### **UNIT I: SECURITY PROBLEM**

Security problem in computing - Characteristics of computers in intrusion- Kinds of security breaches - Points of security vulnerability - Methods of defence - Controls - Effectiveness of controls- Plan of attack encryption.

#### **UNIT II: CRYPTOGRAPHY**

Basic encryption and decryption - Mono alphabetic ciphers- Polyphabetic substitution- Transpositions - Fractional morse - Stream and block ciphers- Characteristics of good ciphers- Secure encryption systems - Public key system- Single key system - Data encryption standard- Rivest - Shamir - Adelman (RSA) encryption.

#### **UNIT III: ROLE OF OPERATING SYSTEM**

Security involving programs and operating systems- Information access problems- program development controls - Operating system controls - Operating system control in use of programs administration control -Protection services for users operating system- Protected objects and method of protection - File protection mechanism - User authentication.

#### **UNIT IV: DATABASE AND NETWORK SECURITY**

Database network security - Security requirements for data base - Reliability and integrity - sensitive data - Interference problem - Multilevel data base - Network security issues- Encryption in networking - Access control - User authentication - Local area networks- multilevel security of network.

#### **UNIT V: COMMUNICATION AND SYSTEM SECURITY**

Communication and system security - Communication characteristics - Communication media- loss of integrity - Wire tapping - electronics mail security - IP security – WEB security - intruders - Viruses - Worms firewalls – Standards

#### ***Course Outcome (CO):***

At the end of this course students will have:

CO1 - To master fundamentals of secret and public cryptography,

CO2 - To master protocols for security services,

CO3 - To be familiar with network security threats and countermeasures,

CO4 - To be familiar with network security designs using available secure solutions (such as PGP, SSL, IPSec, etc),

CO5 - To be familiar with advanced security issues and technologies (such as DDoS attack detection and containment, and anonymous communications,)

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

<i>Course Outcome</i>	Program Outcome												Program Specific Outcome		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
CO1	M	H								M				L	
CO2	M	H						H					L	H	L
CO3			H	M	L				L						M
CO4				H	H						L		H		
CO5						H	H					H			M

H = Highly Related; M = Medium L = Low

**Text Books**

1. William Stallings Cryptography and networks security principles and practice, PHI, 1998
2. Charles, P Pleeger, Security in computing PHI, 1989

**References**

1. Hans, Information and communication security, Springer Verlag, 1998
2. Simonds, Network security, McGraw Hill, 1998
3. Derek Atkins Internet Security , Techmedia, 1998
4. Kernal Texplan, Communication Network Management, PHI, 1992

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*Contact Hours (L-T-P): 3-0-0*

**Hours: 36**

**DATA COMMUNICATION AND COMPUTER NETWORKS**

**Course Objectives:**

1. *Students can understand about the hardware & software commonly used in data communication and networking*
2. *They can gain knowledge about seven layers of the OSI reference model*
3. *Students can compare and contrast WAN and LAN protocols & topologies and their applications.*
4. *Introduction of an advanced element of learning in the field of wireless communication.*
5. *To introduce wireless communication and networking principles, that support the connectivity to cellular networks, wireless networks and sensor devices.*
6. *To understand the use of transaction and e-commerce principles over such devices to support mobile business concepts.*

**Unit I: Introduction**

Signal transmission: Transmission media, signal transmission in channels: Attenuation, distortion and noise source, signal types, signal propagation delay, physical layer interface standards.

**Unit II: Data Transmission**

Data transmission basics, Binary transmission: Parallel transmission, serial transmission, asynchronous transmission, synchronous transmission, transmission control circuits, communication control devices, Error detection and correction methods: Parity, block check sum, CRC error detection schemes for burst errors, Data Compression: Packed decimal, relative encoding, character suppression, Huffman coding, Facsimile compression.

**Unit III: Local Area Network**

LAN topologies, LAN access techniques, bridges, routers.

**Unit IV: Wide Area Network**

Circuit switching, packet switching, frame relay, ISDN fundamentals.

**Unit V: UPPER LAYER PROTOCOLS**

OSI Model, TCP/IP protocols suite, Internet protocol, routing, IP V6, ICMP V6, Transport protocol and application protocols.

***Course Outcome (CO):***

At the end of this course students will have:

CO1 - Understand and be able to explain the principles of a layered protocol architecture; be able to identify and describe the system functions in the correct protocol layer and further describe how the layers interact.

CO2 - Understand, explain and calculate digital transmission over different types of communication media.

CO3 - Understand, explain and solve mathematical problems for data-link and network protocols.

CO4 - Describe the principles of access control to shared media and perform performance calculations.

CO5 - Understand and explain the principles and protocols for route calculations and be able to perform such calculations.

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

<i>Cours e Outco me</i>	Program Outcome												Program Specific Outcome		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	P O9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
CO1	M	H								M				L	
CO2	M	H						H					L	H	L
CO3			H	M	L				L						M
CO4				H	H						L		H		
CO5						H	H					H			M

H = Highly Related; M = Medium L = Low

**Text Books**

1. F.Halsal, “Data Communications, Computer Networks and Open Systems”, Addison - Wesley Publication, Third edition, 1994
2. William Stallings, “Data and Computer Communications”, 5th Edition, Prentice Hall of India, New Delhi, 1997

**References**

1. Jean Walrand, “Communication Networks a first course”, 2nd Edition, McGraw Hill, 1998
2. Lewis Mackenzie, “Communication and Networks”, The McGraw Hill Companies ,1998
3. Andrew.S.Tanenbaum, “Computer Networks”, Prentice Hall of India, 1977
4. Gerd E Keiser “Local Area Networks”, McGraw Hill International Edition

## MOBILE COMPUTING

### Course objectives:

1. *Introduction of an advanced element of learning in the field of wireless communication.*
2. *To introduce wireless communication and networking principles, that support the connectivity to cellular networks, wireless networks and sensor devices.*
3. *To understand the use of transaction and e-commerce principles over such devices to support mobile business concepts.*

### Unit I: Introduction

Introduction to mobile computing - Wireless transmission: propagation, modulation multiplexing, switching, spread spectrum and error control coding.

### Unit II: Wireless Lan

Medium access control and physical layer specifications - IEEE 802.11 - HIPERLAN – Bluetooth.

### Unit III: Wireless Networks

Satellite systems - Cellular networks - Cordless systems - Wireless in local loop - IEEE 802.16.

### Unit IV: Mobile Tcp/Ip And Wap

TCP/IP protocol suite - mobile IP - DHCP - Mobile transport layer - Wireless application protocol.

### Unit V: Mobile Ad-Hoc Networks

Characteristics - Performance issues - Routing algorithms: proactive and reactive - DSDV, AODV, DSR and Hierarchical algorithms.

### *Course Outcome (CO):*

At the end of this course students will have:

CO-1: The students will be able to understand *basic theory and concept of Mobile communication.*

CO2- The student will be able to analyze and understand different generation of mobile communication..

CO-3: The student will be able to analyze and design different standard of communication

CO-4 : The students will able to understand cellular design concepts and various multiple access systems.

CO-5 : The students will able to Describe GSM architecture and protocols.

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

<i>Course Outcome</i>	Program Outcome												Program Specific Outcome		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	H		H			M			M	M	H	M		H	
CO2	H		H	M		H	M			H	M		M	H	M
CO3	H	M						H	H						H
CO4			M			H					M	H	H		
CO5	M	M							L			H			M

H = Highly Related; M = Medium L = Low

**Text Books**

1. J.Schiller, Mobile communications, Addison Wesley, 2000
2. William Stallings, Wireless Communications and Networks, Pearson Education , 2002

## **DIGITAL IMAGE PROCESSING**

### **Course Objectives:**

1. Cover the basic theory and algorithms that are widely used in digital image processing.
2. Expose students to current technologies and issues that are specific to image processing.
3. Develop hands-on experience in using computers to process images.
4. Develop critical thinking about shortcomings of the state of the art in image processing.

### **Unit I: FUNDAMENTALS OF IMAGE PROCESSING**

Introduction – fundamental steps in digital image processing – image sensing and acquisition – sampling and quantization – pixel relationships – color fundamentals and models, file formats, image operations – arithmetic, geometric and morphological - sampling and quantization.

### **Unit II: IMAGE ENHANCEMENT**

Spatial domain - gray level transformations – histogram processing – basics of spatial filtering – smoothing and sharpening spatial filters - frequency domain - filtering in frequency domain – discrete fourier transform, fast fourier transform – smoothing and sharpening filters – homomorphic filtering.

### **Unit III: IMAGE SEGMENTATION AND FEATURE ANALYSIS**

Detection of discontinuities– edge operators– edge linking and boundary detection – threshold– region based segmentation – morphological watersheds– motion segmentation, feature analysis and extraction – spatial techniques.

### **Unit IV: MULTI RESOLUTION ANALYSIS AND COMPRESSIONS**

Multi resolution analysis: image pyramids – multi resolution expansion – wavelet transforms in one dimension - image compression: fundamentals – models – elements of information theory – error free compression – lossy compression – image compression standards

### **Unit V: APPLICATIONS OF IMAGE PROCESSING**

Image classification – image recognition – image understanding – video motion analysis– image fusion – steganography – digital compositing – mosaics – color image processing – string matching – syntactic recognition of strings.

### **Course Outcome (CO):**

At the end of this course students will have:

C0-1: The students will be able to understand *basic theory and algorithms that are widely used in digital image processing* .

CO-2: The student will have the ability to understand the *current technologies and issues that are specific to image processing*

CO3- The student will be able to analyze and develop *hands-on experience in using computers to process images* different antenna.

CO-4: The student will be able to analyze and design different standard of shortcomings *of the state of the art in image processing*

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

Course Outcome	Program Outcome												Program Specific Outcome		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	H		H			M			M	M	H	M		H	
CO2	H		H	M		H	M			H	M		M	H	M
CO3	H	M						H	H						H
CO4			M			H					M	H	H		
CO5	M	M							L			H			M

H = Highly Related; M = Medium L = Low

**Text Book**

1. Jain. K, Fundamentals of Digital Image Processing, Pearson Education, 2003.

**References**

1. Rafael C. Gonzalez and Richard E. Woods, Digital Image Processing, 2<sup>nd</sup> edition, Pearson Education, 2003.
2. Milan Sonka et.al Image Processing, Analysis and Machine Vision, 2<sup>nd</sup> edition, Thomson Learning, 2001.

## Nanotechnology

### **Course Objectives:**

*This course will introduce the basic concepts of nanotechnology to Engineers . This course covets the unique opportunities provided by the nano-scale and focuses on the engineering issues of fabricating and applying structures designed to take advantage of these opportunities. The course begins with defining nanotechnology and nanofabrication. It then moves to the unique features available in nano-scale structures such as large surface-to-volume ratios, quantum size effects, unique chemical bonding opportunities, dominance of physical optics, surface control of reactions and transport, and the creation of structures on the same size scale as basic features in living cells. With this understanding of the uniqueness of the nano-scale, the course progresses into the fabrication methods used in nanotechnology and then into nanostructure applications. The various nanofabrication approaches found in top-down, bottom-up, and hybrid fabrication approaches are explained and discussed in the lecture format. The principles behind the application of structures fabricated at the nano-scale are then addressed in more depth.*

### **Unit I: Atomic structure**

Basic crystallography, Crystals and their imperfections, Diffusion, Nucleation and crystallization, Metals, Semiconductors and Insulators, Phase transformations , Ceramic materials.

### **Unit II: Physical Properties of Materials**

Electrical and Thermal properties, Optical properties of materials, Magnetic properties of materials, Density of states, Coulomb blockade, Kondo effect, Hall effect, Quantum Hall Effect.

### **Unit III: Nanostructures**

Introduction to Nanotechnology, Zero dimensional nanostructures - Nano particles, One dimensional nanostructures - Nano wires and Nano rods.

**Unit IV:** Two dimensional nanostructures - Films, Special nano materials, Nano stuctures fabricated by Physical Techniques, Properties of Nano-materials, Applications of Nano structures, Basics of Nano-Electronics.

### **Unit V: Characterization of Nanomaterials**

SPM Techniques - Scanning Tunneling Microscopy, Atomic Force Microscopy, Magnetic Force Microscopy, Electron Microscopy - Scanning Electron Microscope, Transmission Electron Microscope.

### **Course Outcome (CO):**

At the end of this course students will have:

CO1- Know the processing of Nanoprticles and Nanomaterials and

CO2 - Know the application of Nanotechnology and nanomaterials

CO3 - Describe the basic science behind the properties of materials at the nanometre scale, and the principles behind advanced experimental and computational techniques for studying nanomaterials.

CO4 - Communicate clearly, precisely and effectively using conventional scientific language and mathematical notation.

CO5 - Systematically solve scientific problems related specifically to nanotechnological materials using conventional scientific and mathematical notation

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

<i>Course Outcome</i>	Program Outcome												Program Specific Outcome		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
CO1	M	H								M				L	
CO2	M	H						H					L	H	L
CO3			H	M	L				L						M
CO4				H	H						L		H		
CO5						H	H					H			M

H = Highly Related; M = Medium L = Low

**Text Books**

- 1.Introduction to solid state Physics: C.Kittel
2. Introduction to theory of solids: H.M. Roenberg
3. Physics and Chemistry of materials: Joel I. Gersten
- 4.Handbook of Nanotechnology: Bharat Bhushan(springer)

## EMBEDDED NETWORKS AND PROTOCOLS

### Course Objectives:

1. The objective of this course is to introduce CAN, Concepts of bus access and arbitration, Error processing and management.
2. Familiarization of Ethernet basics with embedded Ethernet exchanging messages using UDP and TCP.
3. To give brief overview of various Industrial Networking Protocol like LIN – local interconnect network, IEEE 1394 etc.
4. To introduce Radio-frequency communication, their internal and external Remote control of opening parts, PKE (passive keyless entry) and passive go, TPMS (tyre pressure monitoring systems).

**Unit I INTRODUCTION TO CAN:** The CAN bus - General - Concepts of bus access and arbitration - Error processing and management - From concept to reality -Patents, licenses and certification - CAN protocol: ‘ISO 11898-1’-Content of the different ISO/OSI layers of the CAN bus- Compatibility of CAN 2.0A and CAN 2.0B.

**Unit II ETHERNET BASICS** Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components – Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol.

**Unit III EMBEDDED ETHERNET** Exchanging messages using UDP and TCP- Serving web pages with Dynamic Data – Serving web pages that respond to user Input -Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

**Unit IV INDUSTRIAL NETWORKING PROTOCOL LIN** – Local Interconnect Network - Basic concept of the LIN 2.0 protocol - Fail-safe SBC – Gateways - Managing the application layers - Safe-by-Wire - Safe-by-Wire Plus - Audio-video buses - I2C Bus - D2B (Domestic digital) bus - MOST (Media oriented systems transport) bus - IEEE 1394 bus or ‘FireWire’- profi bus.

**Unit V RF COMMUNICATION** Radio-frequency communication: internal and external - Remote control of opening parts - PKE (passive keyless entry) and passive go- TPMS (tyre pressure monitoring systems) - Wireless networks- GSM-Bluetooth - IEEE 802.11x - NFC (near-field communication).

### Course Outcome (CO):

At the end of this course students will have:

CO1	Critically evaluate the advantages and disadvantages of selected embedded network standards with regards to performance, reliability, and other metrics.
CO2	Analyse and specify requirements for network technologies based on example application scenarios
CO3	Select suitable network standards based on application requirements
CO4	Implement selected communications protocols as part of a networked embedded system.
CO5	Evaluate the performance of communications protocols used in a networked embedded system.

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

<i>Cours e Outco me</i>	Program Outcome												Program Specific Outcome		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
CO1	M	H								M				L	
CO2	M	H						H					L	H	L
CO3			H	M	L				L						M
CO4				H	H						L		H		
CO5						H	H					H			M

H = Highly Related; M = Medium L = Low

**Text Books:**

1. Dominique Paret , “Multiplexed Networks for Embedded Systems- CAN, LIN, Flexray, Safe-by-Wire...” John Wiley & Sons Ltd- 2007.
2. Jan Axelson ‘Embedded Ethernet and Internet Complete’, Penram publications
3. Glaf P.Feiffer, Andrew Ayre and Christian Keyold, “Embedded networking with CAN and CAN open”. Embedded System Academy 2005.
4. Gregory J. Pottie, William J. Kaiser “Principles of Embedded Networked Systems Design”, Cambridge University Press, Second Edition, 2005.

### **MIXED SIGNAL EMBEDDED SYSTEMS**

#### **Course Objectives:**

*This course includes the knowledge to students different circuits like- analog circuits, mixed signal circuits. It includes knowledge of MOSFET, OPAMP, CMOS amplifier and their different applications. This course also includes the knowledge of ADC, DAC, Phase locked loop and switched capacitor and their applications. In the last unit it gives knowledge of embedded phase locked loop test and synthesizer.*

**Unit I: ANALOG AND MIXED SIGNAL CIRCUITS** Design and verification – applications challenges - market perspective - analog complementary metal oxide semiconductor circuits - current mirrors - current and voltage references - bandgap references.

**Unit II: CMOS AMPLIFIERS** Opamps - high performance complementary metal oxide semiconductor amplifiers – comparators – characterization - two stage open loop comparators - discrete time comparators - high-speed comparators.

**Unit III: SWITCHED CAPACITOR CIRCUITS** Switched capacitor (SC) introduction - offset cancellation - clock feed - through - switched capacitor amplifiers - switched capacitor integrators - switched capacitor filters.

**Unit IV: DAC AND ADC** Introduction - Nyquist rate converters – over sampling converters - pipelined/parallel converters - high speed analog to digital converter design, high speed digital to analog converter design and mixed signal design for radar application - analog to digital converter and digital to analog converter modules used for LIGO.

**Unit V: PHASE LOCKED LOOP** Frequency synthesizers - design of phase locked loop and frequency synthesizers – phase locked loop with voltage driven oscillator – phase locked loop with current driven oscillator – embedded phase locked loop test - phase locked loop synthesizer oscillator by MC14046B.

#### **Course Outcome (CO):**

At the end of this course students will have:

CO1 - In a Position that he/she can design mixed signal based circuits starting from basic constraints to advanced constraints

CO2. Design circuits like switched capacitor circuits, PLL, A/D and D/A converter

CO3. Understand the design of over sampling circuits and higher order modulators

CO4. Should be in a position to design basic cells like OpAmp compensated and high ting against process and temperature variations meeting the mixed signal specifications

CO5. Should be able to design comparators that can meet the high speed requirements of digital circuitry.

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

<i>Course Outcome</i>	Program Outcome												Program Specific Outcome		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
CO1	M	H								M				L	
CO2	M	H						H					L	H	L
CO3			H	M	L				L						M
CO4				H	H						L		H		
CO5						H	H					H			M

H = Highly Related; M = Medium L = Low

**Text Books**

1. Allen, CMOS Analog Circuit Design, Oxford, 2005.
2. Behzad Razavi, Design of Analog CMOS integrated circuit, Tata McGraw Hill, 2004.

**References**

1. Breems, Continuous-Time Sigma Delta Modulations for A/D Conversion, Kluwer, 2002.
2. Michelle Steyaert, Analog Circuit Design, Kluwer, 2003.
3. Gray and Meyer, Analysis and Design of Analog Integrated Circuits, Wiley, 2004.
4. Baker, CMOS Mixed-Signal Circuit Design, Wiley, 2004.

JECRC University

Faculty of Engineering & Technology

*M.Tech. in VLSI & Embedded System Semester III*

*Contact Hours (L-T-P): 4-0-0*

**Hours: 48**

### **MULTIPROCESSOR SYSTEMS-ON-CHIPS**

#### **Course Objectives:**

*This course includes knowledge of system on chip (SOP), challenges in the future, networking on chip (communication using chips) i.e. transmission on chip, architecture of embedded microprocessor, pipelining techniques, performance analysis and modeling of MPSoC architecture and RTOS for MPSoC. This course also includes different applications of MPSoC like Memory Wrapper Generation etc.*

#### **Unit I: FUNDAMENTALS OF MPSoC**

Introduction to SoC - MPSoCs - Challenges - Design Methodologies - Hardware Architectures - Software - Energy-Aware Processor Design - Energy-Aware Memory System Design - Energy-Aware On-Chip Communication System Design - Energy-Aware Software.

#### **Unit II: NETWORKS ON CHIP**

Technology Trends - Signal Transmission on Chip - Micro network Architecture and Control - Software Layers - Architecture of Embedded Microprocessors – Embedded Versus High-Performance Processors A Common Foundation - Pipelining Techniques - Survey of General-purpose 32-bit Embedded Microprocessors - Virtual Simple Architecture (VISA): Integrating Non-Determinism Without Undermining Safety.

**Unit III: PERFORMANCE MODELING AND ANALYSIS FOR MPSoC DESIGN** The Limitations of Traditional ASIC Design - Extensible Processors as an Alternative to RTL - Toward Multiple - Processor SoCs - Processors and Disruptive Technology - Complex Heterogeneous Architectures - Design Challenges - State of the Practice - Chapter Objectives - Structuring Performance Analysis - Architecture Component Performance Modeling and Analysis - Process Execution Modeling - Modeling Shared Resources - Global Performance Analysis.

**Unit IV: ARCHITECTURES AND RTOS FOR MPSoC** On-Chip Communication Architectures - System-Level Analysis for Designing Communication Architectures – Design Space Exploration for Customizing Communication Architectures – Adaptive Communication Architectures– Communication Architectures for Energy/Battery Efficient Systems - Platform Architecture - Tasks - Basics of Scheduling - Basic System Model – Uni-processor Systems - Multiprocessor Systems.

**Unit V: APPLICATIONS BASED DESIGN FOR MPSoC** ASIC to System and Network on Chip - Basics for MPSoC Design Models for Component Abstraction Component - Based Design Environment Memory Wrapper Generation - Component-Based Design of a VDSL Application.

#### ***Course Outcome (CO):***

At the end of this course students will have:

CO1. To learn the basic concepts of NoC design by studying the topologies, router design and MPSoC styles,

- CO2. To learn sample routing algorithms on a NoC with deadlock and livelock avoidance,  
 CO3. To understand the role of system-level design and performance metrics in choosing a NoC design,  
 CO4. To observe the relationship between the requirements and implications of parallel computing/programming tasks on a many-core processor (e.g. with implications on shared/distributed memory system, local vs non-local communication patterns) and the design of a NoC within limited resources,  
 CO5. To understand the relationship between semiconductor technology, computer architecture and computer networking in the design of the communication network for a MPSoC or a many-core design.

**MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

<i>Cours e Outco me</i>	Program Outcome												Program Specific Outcome		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	P O9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
CO1	M	H								M				L	
CO2	M	H						H					L	H	L
CO3			H	M	L				L						M
CO4				H	H						L		H		
CO5						H	H					H			M

H = Highly Related; M = Medium L = Low

**Text Book**

- Wayne Wolf, “Multiprocessor Systems-on-Chips”, Morgan Kaufmann Publishers, 2005.

**Reference**

- Joseph A. Fisher, Paolo Faraboschi and Cliff Young, “Embedded Computing” Morgan Kaufmann Publishers, 2005.

## **Dissertation**

### **Subject Objectives:**

The objective of this subject is to provide exposure to the current technology by devoting 1 year for project in the interest area of students according to current research areas in electronics and communication engineering. This project can be done in any industry or in the university campus under the guidance of faculty of Electronics and Communication Engineering department.